Low power Full Swing SRAM Architecture with Power gating

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Abstract : **Low power & speedy memory design has big impact in SOC devices & its applications. Hence SRAM architecture is designed in the manner of low power consumption or reduced power leakages. To reduce power leakages in SRAM architecture power gating techniques can be used. Which reduces the leakage through the CMOS transistors. In the case of average-9T SRAM architecture, a full-swing local bit line (BL) that is connected to the gate of the read buffer can be achieved with a boosted word line (WL) voltage. Thus, a full-swing local BL cannot be achieved, and the gate of the read buffer cannot be driven by the full supply voltage (VDD), resulting in a considerably large read delay. In the proposed SRAM architecture, full swing of the local BL is ensured by the use of cross-coupled PMOSs, and the gate of the read buffer is driven by a full VDD, without the need for the boosted WL voltage. This SRAM architecture is implemented in Tanner EDA tool.**

1. INTRODUCTION

The portable devices such as hand held mobile devices and personal digital assistants are gaining more popularity as well as making changes in every aspect of our daily lives. The major concern enhancing the demand for portable device market is multimedia data processing, which includes the image/video applications .video applications require a large amount of embedded memory access, which results in significant power consumption and thus limits the battery life time. Power dissipation has become an important consideration due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. Low power design is a, buzzword these days and designing with low power requirements has been always an important aspect of video applications. The overarching reason why the low power design is becoming so important today is the increase of leakage current with the shrinkage of device dimension. Low power design is indispensible to realize battery operated systems. Due to the limited size of handheld devices, it is impossible to use larger batteries in it and short battery life time of a smaller battery limits the use of them.

One of the effective ways to reduce the dynamic power consumption is lowering the operating voltage due to its quadratic relationship. In scaled technologies maintaining high SRAM yield becomes more challenging since they are particularly vulnerable to process variations due to the minimum sized devices used in SRAM bit cells . This section revolves round the performance comparison of SRAM cells consisting of various varieties of transistors wont to store single bit. From last four decades, we have a tendency to square measure cutting down the CMOS devices to realize the higher performance in terms of speed, power consumption, noise margins, delay etc. SRAM based mostly cache recollections square measure ordinarily used because of their higher speed. However because of device scaling we have a tendency to face style challenges for micro millimeter SRAM style.

Owing to low threshold voltage and extremist skinny gate compound, the outpouring energy consumption is obtaining increased. The info stability throughout browse and write operation is additionally obtaining affected. There's another issue like random dopant fluctuation, line edge roughness and compound thickness fluctuation that decreases the soundness of SRAM cell. During this section performance analysis of 6T, 8T and 9T has been carried power consumption and delay.

2. EXISTING SYSTEM

To address the read destructive problem, the read and write operations are separated by adding transistor stack to the conventional 6T SRAM cell, thus it has the area penalty but operates efficiently than the 6T SRAM cell at lower . The 8T SRAM circuit described in this section . The schematic of the 8T SRAM cell with transistors sized for a 65-nm CMOS technology.

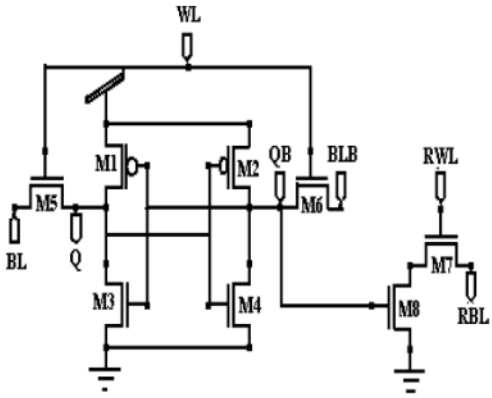

Figure 1 8TSRAM Cell

The disturbance of bit lines during read operation is the primary source of instability problem in SRAM operation.

The stability in 8T SRAM cell can be enhanced by isolating the read port from the write bit lines. The 8T SRAM cell composed of conventional 6T SRAM cell for writing operation and a transistor stack, which can be used for read operation. The read and write operations are controlled by separate signals Write Word Line (WWL) and Read Word Line (RWL). During the read operation Read Bit Line (RBL) is pre charged to and WWL is maintained at Depends on the value stored in

cross coupled inverters RBL, discharges (or) maintained at. If RBL discharges, it can be treated as the stored bit is „1", otherwise it is „0". The storage nodes are completely isolated from the write bit lines, which can increases the stability of the SRAM cell.

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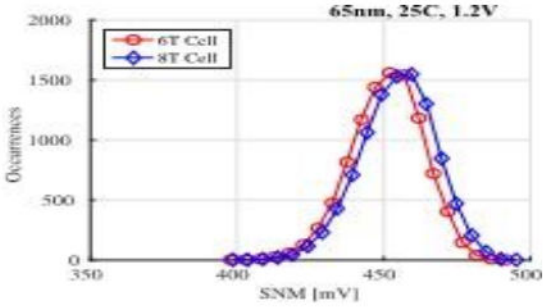

Figure 2 Hold State

During the write operation WBL and WBLB lines are pre charged to predetermined values. Then, asserting the write word line WWL and nodes attain the corresponding values from the bit lines.

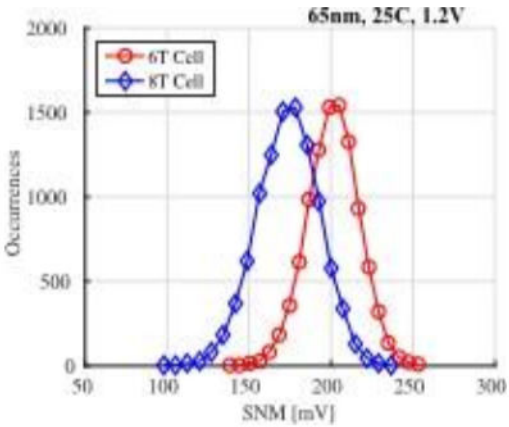

Figure 3 Read State

It uses the two additional Word Lines to perform read and write operations, when compared with 6T SRAM cell, which could increase the metal density, wire delay and dynamic power consumption and leakage power.

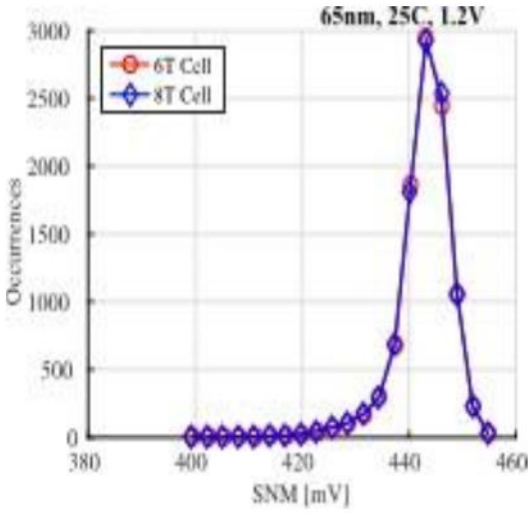

Figure 4 Write State

The primary mechanism that enables an LPA attack on a conventional 6T SRAM cell is the asymmetrical leakage currents of the cell in hold mode, depending on the stored data and the BL/BLB voltages.

To avoid this asymmetry and produce a similar standby current pattern for both data levels, we propose an 8T SRAM cell implementation, previously used for improved read speed.

The 8T cell is based on a conventional 6T cell with two additional nMOS transistors (M7 and M8). These transistors are similar to the access transistors (M2 and M5) and are connected between BL and QB, and BLB and Q, respectively. The gate of M7 and M8 is connected to GND, to keep them in cutoff throughout all the memory operating modes. Nonetheless, during standby, these transistors result in two additional leakage current paths in the case where the voltages in Q and BL are equal.

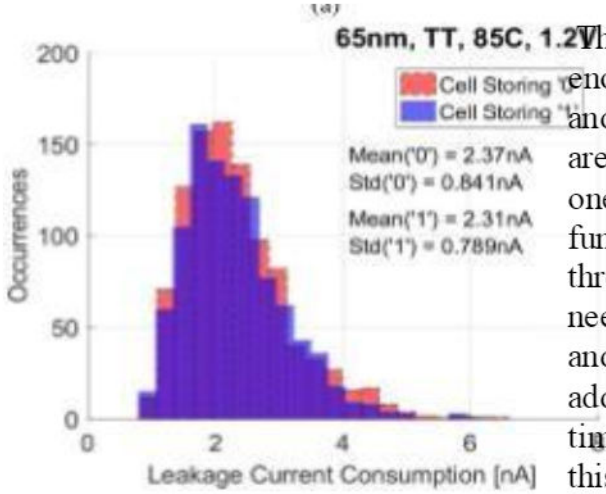

Figure 5 Leakage Current Distribution of 8T SRAM Cell

As a result of this symmetry, the number of leakage current paths becomes equal under any BL/BLB condition for both data levels stored in the cell. , showing the leakage current paths for both cases, where the cell stores "1" and a "0."

As expected, the leakage current distributions for both data levels had a substantially smaller mean difference than a similar distribution for a 6T cell. The mean leakage currents for cells storing "0" and "1" were 2.37 and 2.31 nA, respectively.

3. PROPOSED SYSTEM

The proposed architecture only one unmarried bit line capacitance (BL) will be charged and discharged throughout write operation which leads to important reduction in dynamic electricity intake and at the identical time the records stability of the 9T SRAM cell as in is likewise maintained.

The planned mobile keeps enormously greater write margins and functionality, even if the PMOS are lots more potent than the NMOS ones. This mobile finishes full functionality deep into the sub threshold section deprived of the need for special marginal circuits and techniques that require additional strength, die area and timing schemes [6].In calculation, this circuit presents a low-leakage nation, at which its static power is lower than any of the other enactments whilst operated at a comparable supply voltage . This is carried out lacking any enactment degradation, even as safety a reasonable SNM. A 9T SRAM cell enhances the data stability and

reduces leakage power consumption. The access transistors are controlled by the word line signal(WL). These access transistors connect the bit line to store the value of nodes. Nonetheless, during standby, these transistors result in two additional leakage current paths in the case where the voltages in Q and BL are equal. This cell employs two more transistors to access the read bit line. Write access to the cell occurs through the write access transistors and from the write bit lines, BL and BLB. (BL) will be charged and discharged during write operation which results in major reduction in dynamic power ingestion and at the same time the data stability of the 9T SRAM cell as in is also maintained. Two write access transistors organized by a write signal (WR) connected to bit line (BL) and bit line bar (BLB). Here only one single bit line capacitance (BL) will be charged and discharged during write operation which results in important reduction in dynamic power consumption and at the equal time the data stability of the 9T SRAM cell as in is also maintained. Here only one single bit line capacitance (BL) will be charged and discharged during write operation which results in important reduction in dynamic power consumption and at the equal time the data stability of the 9T SRAM cell as in is also maintained. Here only one single bit line capacitance (BL) will be charged and discharged during write operation which results in important reduction in dynamic power consumption and at the equal time the data stability of the 9T SRAM cell as in is also maintained. This architecture uses a read decoupled access buffer and power grating transistors to execute reliable read and write operations. It uses bit interleaving to achieve soft error immunity and utilizes a column-based virtual VSS signal.

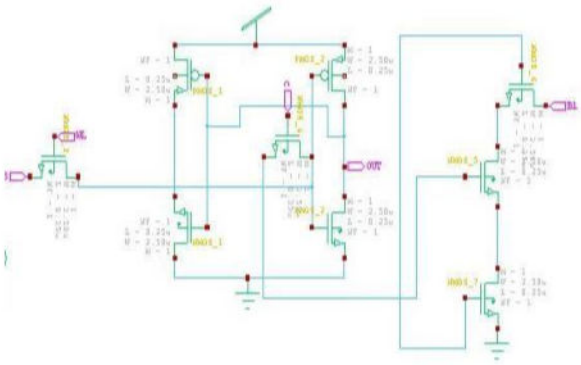

Figure 6 9TSRAM Cell

Two write access transistors organized by a write signal (WR) connected to bit line (BL) and bit line bar (BLB). Here only one single bit line capacitance (BL) will be charged and discharged during write operation which results in important reduction in dynamic power consumption and at the equal time the data stability of the 9T SRAM cell as in is also maintained.

4. COMPARISION BETWEEN 8T & 9T

The dissertation work revolves around the performance comparison of SRAM cells consisting of different number of transistors used to store single bit. SRAM stands for static random access memory. It is a type of semi-conductor memory which uses bi-stable latching circuitry to store single bit [1].

S.NO	POWER MEASUREMENT
6T METHOD	4.099
8T METHOD	9.1214
9T METHOD	1.603

Table 1 Power Measurement

The word static here points that it needs not to be refreshed periodically unlike dynamic random access memory. Sram exhibits data-remanence but still it can be called volatile memory as it eventually loses the data when memory is not powered.

From last four decades, we are scaling down the CMOS devices to achieve the better performance in terms of speed, power consumption, noise margins, delay etc. Sram based cache memories are commonly used due to their higher speed. But due to device scaling we are facing design challenges for nanometre sram design.

S.NO	DELAY
6 T METHOD	3.4291
8T METHOD	4
9T METHOD	1.996

Table 2 Delay Measurment

Because of low threshold voltage and ultra thin gate oxide, the leakage energy consumption is getting increased. The data stability during read and write operation is also getting affected [5]. There aresome other factor like random dopant fluctuation, line edge roughness and oxide thickness fluctuation

After comparing the 6T and 8T SRAM cell ,it is found that 6T sram cell provide a very low write delay nearly 7 times lesser when compared to 8T SRAM cell. While in case of read delay there is less difference, read delay of 8T SRAM is nearly 1.35 times higher as compared of to 6T SRAM. The power dissipation of 6T sram is half of power dissipated in 8T SRAM. This is due to more number of transistor in 8T SRAM and secondly little complex working than other one. In case of 9T SRAM the write delay as compared 6T SRAM is nearly equal. The width of the transistor also affects the delay but we can't extend width too much as it increases the area of the SRAM cell.

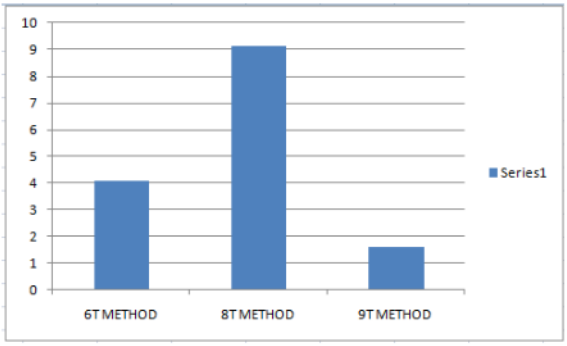

Figure 7 Power Measurement Chart

While talking about the results of 9T SRAM, we see that the read delay of this SRAM is little bit high as compared to 8T SRAM and nearly 1.45 higher than 6T SRAM's read delay. Read delay is maximum in case of this cell because it uses the high voltage transistor which increases the delay but it improves the driving capability. Performance is improved in case of this cell. If we notice the write delay, it is almost equal to 6T SRAM write delay. The 9T SRAM structure uses

the advantages of 6T and 8T SRAM, 9T SRAM uses the two bit lines and also have the different read and write line. From results it looks like that 6T SRAM is the better one out of three but that is not right. Because there some other factor also on which performance of these cell depends. Data retention voltage is one out them. From the theoretical study and literature survey it is found 9T SRAM have low data retention voltage out of three cells.

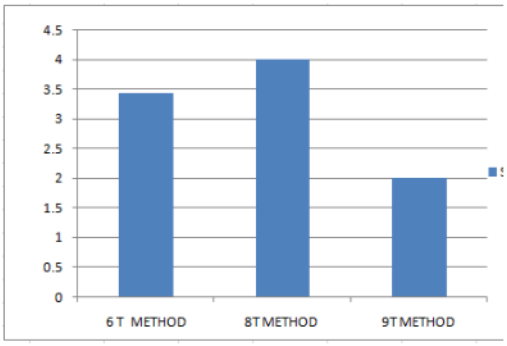

Figure 8 Delay Measurement Chart

5. AREA COMPARISION

In order to evaluate the area overhead of the proposed 8T SRAM cell over a conventional 6T cell, both cells were implemented in a 65-nm CMOS technology with minimal sized devices. Fig. 8 shows the layout views of the proposed 8T cell and the conventional 6T cell, implemented with the standard design rules. All the polylines are routed horizontally without bends, complying with the thincell requirements for deeply scaled process nodes. Measured at 1.33 μm×1.57 μm (2.08 μm2), the 8T cell features GND, VDD, and WL lines routed in M3, and BL and BLB lines routed in M4. A redrawn 6T SRAM cell was measured at 2.19 μm × 0.67 μm (1.46 μm2), which is 30% smaller than the proposed 8T cell.

6. CONCLUSION

Embedded memories implemented with 6T SRAM macros occupy a large portion of cryptographic systems and may hold secret data; these require special design steps to provide resiliency to leakage power attacks. In this brief, we provide an in-depth analysis of the leakage dependence on the stored data of a 6T SRAM array. A leakage power attack is illustrated on a 6T SRAM array, and achieved successful data extraction through leakage current measurements to prove its unreliability for security applications. Low power & speedy memory design has big impact in SOC devices & its applications.

9T SRAM asymmetric architecture is designed in the manner of low power consumption or reduced power leakages using 25nm CMOS technology. To perform differential power analysis of 6T SRAM cell, 8T SRAM cell and 9T SRAM cell. To design layout for 6T SRAM cell, 8T SRAM cell and 9T SRAM cell. To simulate and calculate various performance metrics such as area, power and delay. Thus, a full-swing local BL cannot be achieved, and the gate of the read buffer cannot be driven by the full supply voltage (VDD), resulting in a considerably large read delay. In the proposed SRAM architecture, full swing of the local BL is ensured by the use of cross coupled PMOSs, and the

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7. REFERENCES

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