A THREE STAGE SELF BALANCED FLYING CAPACTIOR AND H BRIDGE TOPOLOGY FOR 17 LEVEL INVERTER

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ABSTRACT: **A multilevel inverter for generating 17 voltage levels using a three-level flying capacitor inverter and cascaded H-bridge modules with floating capacitors has been proposed. a new method of generating higher number of levels in the voltage waveform by stacking multilevel converters with lower voltage space vector structures is proposed. An important feature of this stacked structure is the use of low voltage devices while attaining higher number of levels. These will find extensive applications in electric vehicles since direct battery drive is possible. The stability of the capacitor balancing algorithm has been verified both during transients and steady state operation. All the capacitors in this circuit can be balanced instantaneously by using one of the pole voltage combination Additional advantage is, if one of the H-bridges fail, the inverter can still be operated at full load with reduced number of levels. This configuration has very low dv/dt and common mode voltage variation.**

Keywords:Multilevel converter,H-bridge,Matlab

1. Introduction:

Basically Inverter is a device that converts DC power to AC power at desired output voltage because of other advantages such as high power quality , lower order harmonics, lower switching losses, and better electromagnetic interference, and frequency. Demerits of inverter are less efficiency , high cost, and high switching losses. To overcome these demerits, were going to multilevel inverter. Multilevel inverter output voltage produce a star case output waveform, this waveform look like a sinusoidal waveform. The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero. The multilevel inverters are mainly classified as Di ode clamped, Flying capacitor inverter and cascaded multi level inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor. Moreover, abundant modulation techniques have been developed in cascade multilevel inverter and reducing the power losses.

Features of multilevel inverters

1. They can generate output voltages with extremely low distortion and lower order harmonics.

2. They draw input current with very low distortion.

3. In addition, using sophisticated modulation types of methods, CM voltage can be eliminated.

4. They can operate with a less switching frequency.

POWER CIRCUIT TOPOLOGY

The proposed converter is a hybrid multilevel topology employing a three-level flying capacitor inverter and cascading it with three floating capacitor H-Bridges.

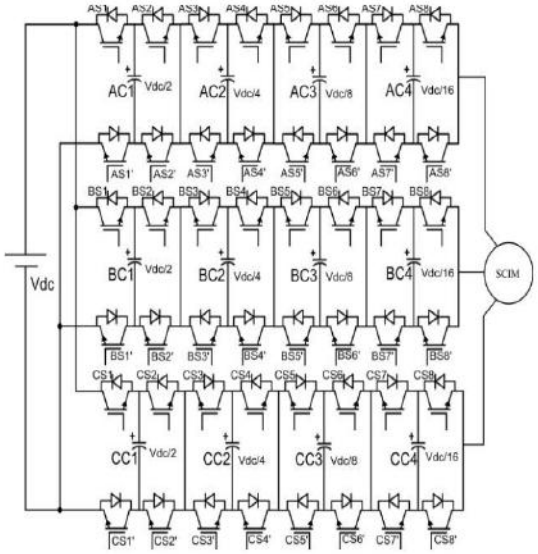


Fig. 1.1.Three-phase power schematic of the proposed seventeen-lever inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a Single DC link.

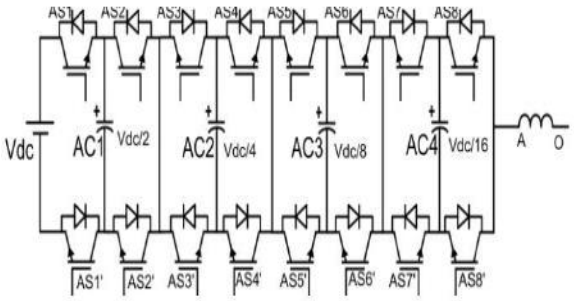


Fig. 1.2.One phase of the proposed seventeen-lever inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single DC link.

The three-phase power schematic is shown in Fig.11. The voltages of capacitorsAC1, BC1 and CC1 are maintained at Vdc/2. Capacitors AC2,BC2 and CC2 are maintained at voltage level of Vdc/4.Similarly capacitors AC3, BC3 and CC3 are maintained at voltage level of Vdc/8 and capacitors AC4, BC4 and CC4 are maintained at voltage level of Vdc/16. Each cascaded H-bridge can either add or subtract its voltage to the voltage generated by its previous stage. In addition to that, the CHBs can also be by passed. The resulting inverter pole voltage is the arithmetic sum of voltages of each stage. The schematic diagram for one phase of the proposed converter is shown in Fig. 1.2. The switch pairs (AS1, AS1'), (AS2, AS2'), (AS3 AS3'), (AS4, AS4'),(AS5, AS5'), (AS6, AS6'), (AS7, AS7') and (AS8, AS8') are switched in complementary fashion with appropriate dead time .Each switch pair has two distinct logic states, namely top device is ON (denoted by 1) or the bottom device is ON(denoted by 0). Therefore, there are 256 (28) distinct switching combinations possible. Each voltage level can be generate during one or more switching states (pole voltage redundancies).

TABLE.1

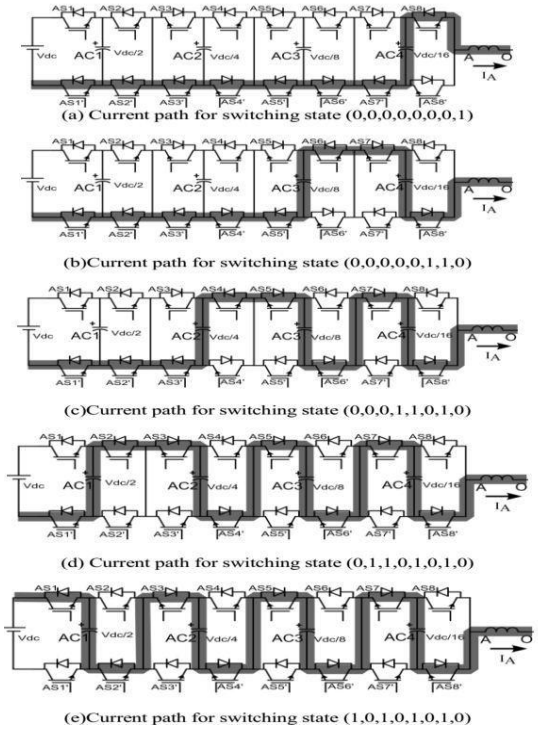
Pole voltage redundancies and capacitor states for various switching combinations when pole sources current

S.No	Pole Voltage	Switch State (S1,S2,S3,S4,S5,S6,S7,S8)	C1'	C2'	C3'	C4'
1	0	(0,0,0,0,0,0,0,0)	0	0	0	0
2	Vdc/16	(0,0,0,0,0,0,1,1)	0	0	0	-
3		(0,0,0,0,0,1,1,0)	0	0	-	+
4		(0,0,0,1,1,0,1,0)	0	-	+	+
5		(0,1,1,0,1,0,1,0)	-	+	+	+
6		(1,0,1,0,1,0,1,0)	+	+	+	+
7	Vdc/8	(0,0,0,0,1,1,0,0)	0	0	-	0
8		(0,0,0,1,1,0,0,0)	0	-	+	0
9		(0,1,1,0,1,0,0,0)	-	+	+	0
10		(1,0,1,0,1,0,0,0)	+	+	+	0
11	3Vdc/16	(0,0,0,0,1,1,0,1)	0	0	-	-
12		(0,0,0,1,1,0,0,1)	0	-	0	+
13		(0,0,0,1,1,0,1,1)	0	-	+	-
14		(0,1,1,0,0,0,1,0)	-	+	0	+
15		(0,1,1,0,1,0,0,1)	-	+	+	-
16		(1,0,1,0,0,0,1,0)	+	+	0	+
17		(1,0,1,0,1,0,0,1)	+	+	+	-
18	Vdc/4	(0,0,0,1,0,0,0,0)	0	-	0	0
19		(0,1,1,0,0,0,0,0)	-	+	0	0
20		(1,0,1,0,0,0,0,0)	+	+	0	0
21	5Vdc/16	(0,0,0,1,0,0,0,1)	0	-	0	-
22		(0,0,0,1,0,1,1,0)	0	-	-	+
23		(0,1,0,0,1,0,1,0)	-	0	+	+
24		(0,1,1,0,0,0,0,1)	-	+	0	-
25		(0,1,1,0,0,1,1,0)	-	+	-	+
26		(1,0,0,0,1,0,1,0)	+	0	+	+
27		(1,0,1,0,0,0,0,1)	+	+	0	-
28		(1,0,1,0,0,1,1,0)	+	+	-	+
29	3 Vdc/8	(0,0,0,1,1,0,1,0)	0	-	-	0
30		(0,1,0,0,1,0,0,0)	-	0	+	0
31		(0,1,1,0,0,1,0,0)	-	+	-	0
32		(1,0,0,0,1,0,0,0)	+	0	+	0
33		(1,0,1,0,0,1,0,0)	+	+	-	0
34	7 Vdc/16	(0,0,0,1,0,1,0,1)	0	-	-	-
35		(0,1,0,0,0,1,0,0)	-	0	0	+
36		(0,1,0,0,1,0,0,1)	-	0	+	-
37		(0,1,1,0,0,1,0,1)	-	+	-	-
38		(1,0,0,0,0,1,0,0)	+	0	0	+
39		(1,0,0,0,1,0,0,1)	+	0	+	-
40		(1,0,1,0,0,1,0,1)	+	+	-	-
41	Vdc/2	(0,1,0,0,0,0,0,0)	-	0	0	0
42	Vdc/2	(1,0,1,0,0,0,0,0)	+	0	0	0
43	9 Vdc/16	(0,1,0,0,0,0,0,1)	-	0	0	-
44		(0,1,0,0,0,1,1,0)	-	0	-	+
45		(0,1,0,1,1,0,1,0)	-	-	+	+
46		(1,0,0,0,0,0,0,1)	+	0	0	-
47		(1,0,0,0,0,1,1,0)	+	0	-	+
48		(1,0,0,1,1,0,1,0)	+	-	+	+
49	5 Vdc/8	(1,1,1,1,1,0,1,0)	0	+	+	+
50		(0,1,0,0,0,1,0,0)	-	0	-	0
51		(0,1,0,1,1,0,0,0)	-	-	+	0
52		(1,0,0,0,0,1,0,0)	+	0	-	0
53		(1,0,0,1,1,0,0,0)	+	-	+	0
54		(1,1,1,0,1,0,0,0)	0	+	+	0
55	11 Vdc/16	(0,1,0,0,0,1,0,1)	-	0	+	-
56		(0,1,0,1,0,0,1,0)	-	-	0	+
57		(0,1,0,1,1,0,0,1)	-	-	+	-
58		(1,0,0,0,0,1,0,1)	+	0	-	-
59		(1,0,0,1,0,0,1,0)	+	-	0	+
60		(1,0,0,1,1,0,0,1)	+	-	+	-
61		(1,1,1,1,0,0,1,0)	0	+	0	+
62	3 Vdc/4	(1,1,1,0,1,0,0,1)	0	+	+	-
63		(0,1,0,1,0,0,0,0)	-	-	0	0
64		(1,0,0,1,0,0,0,0)	+	-	0	0
65		(1,1,1,0,0,0,0,0)	0	+	0	0
66	13 Vdc/16	(0,1,0,1,0,0,0,1)	-	-	0	-
67		(0,1,0,1,0,1,1,0)	-	-	-	+
68		(1,0,0,1,0,0,0,1)	+	-	0	-
69		(1,0,0,1,0,1,1,0)	+	-	-	+
70	7 Vdc/8	(1,1,0,1,0,1,0,1)	0	0	+	+
71		(1,1,1,1,0,0,0,1)	0	+	0	-
72		(1,1,1,1,0,1,1,0)	0	+	-	+
73		(0,1,0,1,0,1,0,0)	-	-	-	0
74		(1,0,0,1,0,1,0,0)	+	-	+	0
75	15 Vdc/16	(1,1,0,1,0,1,0,0)	0	0	+	0
76		(1,1,1,0,0,1,0,0)	0	+	-	0
77		(0,1,0,1,0,1,0,1)	-	-	-	-
78		(1,0,0,1,0,1,0,1)	+	-	-	-
79		(1,1,0,0,0,0,1,0)	0	0	0	+
80		(1,1,0,0,1,0,0,1)	0	0	+	-
81		(1,1,1,0,0,1,0,1)	0	+	-	-
82	Vdc	(1,1,0,0,0,0,0,0)	0	0	0	0

Symbols of + , - and 0 indicates the capacitor is charging, discharging and no effect respectively for positive direction of current

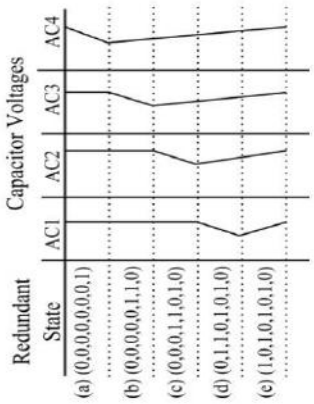
By switching through the redundant switching combinations(for the same pole voltage), the current through capacitors can be reversed and their voltages can be controlled to their prescribed values. This method of balancing the capacitor voltages at all load currents and power factors instantaneously has been observed for 17 pole voltage levels. They are 0,Vdc/16, Vdc/8, 3Vdc/16, Vdc/4, 5Vdc/16, 3Vdc/8, 7Vdc/16,Vdc/2, 9Vdc/16, 5Vdc/8, 11Vdc/16, 3Vdc/4, 13Vdc/16,7Vdc/8, 15Vdc/16 and Vdc. However, by

switching through all the possible pole voltage switching combinations, 31 distinct pole voltage levels can be generated using the proposed topology. In the additional 14 levels, the voltages of capacitors can be balanced only in a fundamental cycle. 3Vdc/16, Vdc/4, 5Vdc/16, 3Vdc/8, 7Vdc/16,Vdc/2, 9Vdc/16, 5Vdc/8, 11Vdc/16, 3Vdc/4, 13Vdc/16,7Vdc/8, 15Vdc/16 and Vdc. However, by switching through allthe possible pole voltage switching combinations, 31 distinct pole voltage levels can be generated using the proposed topology. In the additional 14 levels, the voltages of capacitors can be balanced only in a fundamental cycle. There are 82 switching combinations (Table. 3.1) that can be used to generate the above mentioned 17 pole voltage levels where instantaneous capacitor voltage balancing is possible. The effect of 82 switching combinations on every capacitor's charge state (charge or discharge) for positive direction of current . For negative direction of current, the effect of the switching state on the capacitor is reversed. For example, when the controller demands a pole voltage of Vdc/16, there are 5 different redundant switching combinations to generate it. Each switching combination has a different effect on the state of charge of the capacitors. When the switching state (0,0,0,0,0,0,0,1) (Table. 1.1) is applied, the capacitor C4 discharges when the pole is sourcing current To balance the capacitor C4 and to bring its voltage back to the prescribed value (Vdc/16), one of the other 4switching combinations is applied . It can be observed that when switching state (0,0,0,0,0,1,1,0) is applied ,the direction of current in the capacitor C4 is reversed and the capacitor C4 charges. However in this process, the capacitor C3 is discharge switching state redundancy of (0,0,0,1,1,0,1,0) is applied which discharges C2. To charge C2 one of the switching redundancies is applied based on the state of charge of capacitor C1. If switching state (0,1,1,0,1,0,1,0) is applied, the capacitor C1 is discharged and this state charges all the other capacitors. Lastly, when switching state of(1,0,1,0,1,0,1,0) is applied, all the 4 capacitors are charged for positive direction of current as shown in Fig. 3.3(e).By switching through the redundant pole voltage combinations, It can be observed that the all the capacitors' voltages can be maintained at their prescribed values while generating pole voltage of Vdc/16 for positive direction of current. If all the capacitors need discharging, the capacitor C4 is discharged first and the remaining capacitors can be discharged during subsequent switching cycles when C4 d. If the capacitor C3 needs charging, switching state needs to be charged. For negative direction of current the effect of the capacitor voltages is the opposite. The entire process of capacitor voltage balancing for pole voltage of Vdc/16 that has been explained is illustrated in Fig. 4.4. Here the capacitor voltage variation with application of various redundant states for pole voltage of Vdc/16 has been shown for positive direction of current. For other pole voltages namely, Vdc/8, 3Vdc/16, Vdc/4, 5Vdc/16 3Vdc/8, 7Vdc/16, Vdc/2, 9Vdc/16, 5Vdc/8, 11Vdc/16, 3Vdc/4,13Vdc/16, 7Vdc/8, 15Vdc/16 and Vdc, a similar strategy can be used to balance all the capacitor voltages.



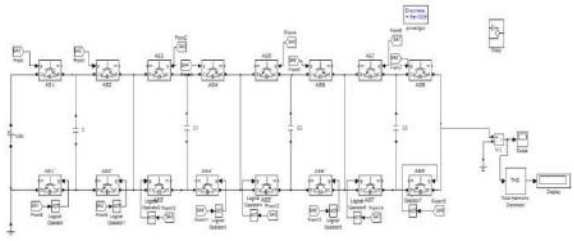
switching Redundancies for pole voltage of Vdc/16

The switching frequency of any CHB module is at most the PWM switching frequency of the converter. This is due to the synchronization of application of the switching state with every PWM transition(the switching state is latched till the next PWM transition).Moreover in this scheme, only the capacitors that contribute to the output pole voltages are switched.

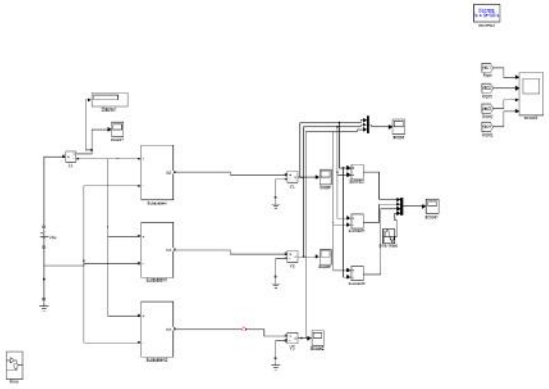


Capacitor voltage variation with application of redundant states forpole voltage of Vdc/16 for positive current

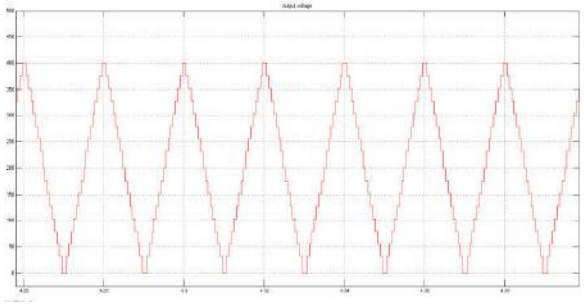
Proposed Method



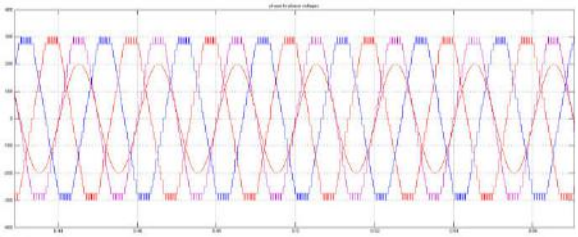
Simulation diagram for the proposed inverter. It is hybrid multilevel topology employing a three-level flying capacitor inverter and cascading git with three floating capacitor H-Bridges.



Simulation diagram of 3 phase inverter.



17 level output voltage for the proposed inverter.



phase to phase output voltage

Comparison Table

The table mentioned below represents the comparison between existing and proposed system.

	Existing System	**Proposed System**
No. Of Switches	18	16
No. Of Sources	2	1
Output Levels	9	17
Topology	Stacked Multilevel Inverter(Flying Capacitor+ H-Bridge)	Flying Capacitor + floating capacitor H-Bridge
Algorithm	Hysteresis Based Capacitor voltage balancing algorithm	Space vector control algorithm

Conclusion

A multilevel inverter that operates in a single dc and the minimum number of switches has been proposed. The capacitor balancing modulation technique for the proposed scheme has been generated and validated to generate the multilevel pattern. The multilevel generated contains a three capacitors that balancing the voltage is done through the PWM modulation. This inverter uses a single dc sources and reduced number of dc sources which are minimal compared to the existing schemes, and also it can provides an additional space to modify the number of levels without touching the main circuit, with the addition of sub blocks and the capacitors the voltage level addition can be included and the addition of the such voltage levels without any modification in the modulation scheme too. As the system has the minimal switches the requirement of the hardware drivers are being reduced Therefore, construction cost of the proposed multilevel inverter is lower and it is not bulky.

Future scope:

The Multilevel as the form contain minimal number of switches compared to the conventional H bridges and uses a single dc source, which can be used to integrate renewable sources are the major needs to adopt renewable sources, further in order to extend their operation in the renewable sources the inverters can be modified as the Z source inverters which may require the voltage boosting capabilities in the un consistent states for the renewable sources. Extending the inverter towards the renewable systems variations and operating in to reliable states would be the extension to the current form.

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