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UNIT - V

POWER DEVICES AND DISPLAY DEVICES

UJT, SCR, Diac, Triac, Power BJT - Power MOSFET - DMOS - VMOS, LED, LCD, Photo transistor, Opto Coupler, Solar cell, CCD.

IMPORTANT ANNA UNIVERSITY QUESTIONS

* Intrinsic stand off Ratio **- 2 Marks**
* UJT - Working, Construction, Characteristics, Applications **- 8 Marks**
* SCR - Working, Construction, Characteristics, Applications **- 16 Marks**
* DIAC + TRIAC **- 8+8 Marks**
* LED Vs LCD **- 2 Marks**
* Solar Cells - **2 Marks , 8 Marks**

5.1 UJT (UNIJUNCTION TRANSISTOR)

(Nov/Dec 2008 - 8 Marks, May/June 2010 -16 Marks, May /June 2012 - 8 Marks, Nov/Dec 2012 - 8 Marks)

→ Three terminal device

→ Consists of slab of lightly doped n- type silicon material with two - end terminals B_1 (base - 1) and B_2(base -2)

→ Heavily doped p-type material is injected to one side of bar which produces **p-n junction.**

Monograph On Power Devices and Display Devices
Christo Ananth,
Assistant Professor, Department of ECE, Francis Xavier Engineering College, Tirunelveli, India

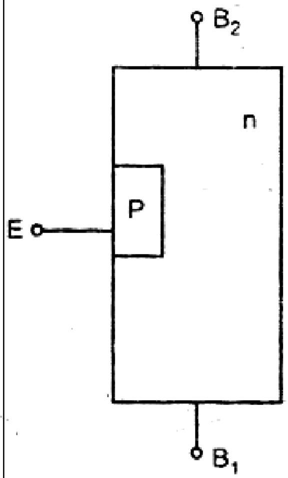


Fig 5.1 Construction of UJT

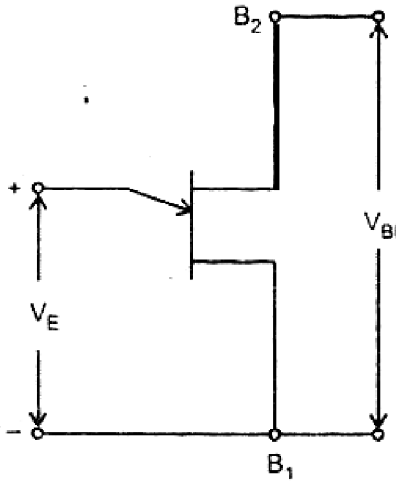


Fig 5.2 Symbol of UJT

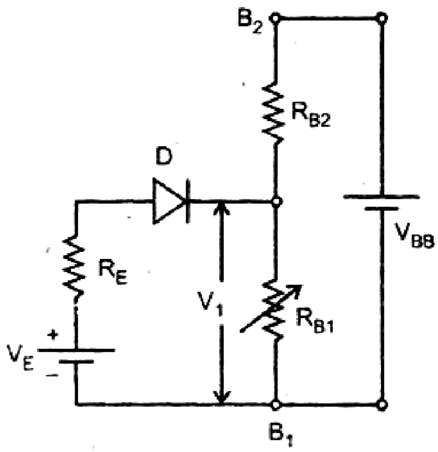


Fig 5.3 Equivalent circuit of UJT

→ Terminal connected to p-n junction is termed as **EMITTER (E)**

→ n - type silicon has a resistance which are represented as two resistors R_{B1} and R_{B2} in series.

→ R_{B2} →fixed; R_{B1}→ Variable.

→ pn junction is represented by diode.

→ When emitter diode is non-conducting (when $I_E = 0$), resistance between bases B_1 and B_2 is sum of R_{B1} and R_{B2}.

$$\boxed{R_{BB} = R_{B1} + R_{B2}} \approx (5 - 10)\,K\Omega$$

$$V_1 = V_{BB}\frac{R_{B1}}{R_{B1} + R_{B2}}$$

$$= V\frac{R_{B1}}{R_{BB}} \quad (\because R_{BB} = R_{B1} + R_{B2})$$

$$\boxed{V_1 = \eta V}$$

where $\eta = \frac{R_{B1}}{R_{BB}} =$ **intrinsic standoff ratio** $(0.5 - 0.8)$

5.1.1. WORKING: (Nov /Dec 2008 -2 Marks) (May/June 2009 - 2 Marks)

* When applied voltage at Emitter is 0, reverse saturation current I_{EO} flows.

* Voltage $V_1 = \eta V_{BB}$ appears across emitter diode.

* When Voltage $V_E > V_1$ by forward voltage drop of diode ($V_E > V_1$+0.7) is applied, then diode conducts.

* Voltage at which diode conducts is called as "**PEAK VOLTAGE**"

$$\boxed{V_p = \eta V_{BB} + V_D}$$

* Corresponding current is called as "**PEAK CURRENT**"**(I_p)**

* When pn junction is forward biased, charge carriers are injected into R_{B1} region which decreases the resistance R_{B1}.

* So, Voltage drop across R_{B1} decreases which causes pn junction to be more heavily forward biased. This produces greater forward current.

* More charge carriers are injected to R_{B1} region increasing emitter current I_E.

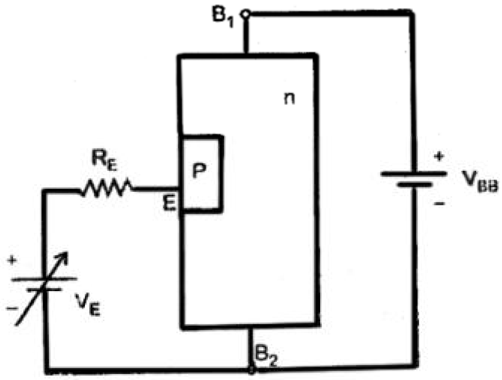


Fig 5.4 UJT with bias

5.1.2 CHARACTERISTICS OF UJT:

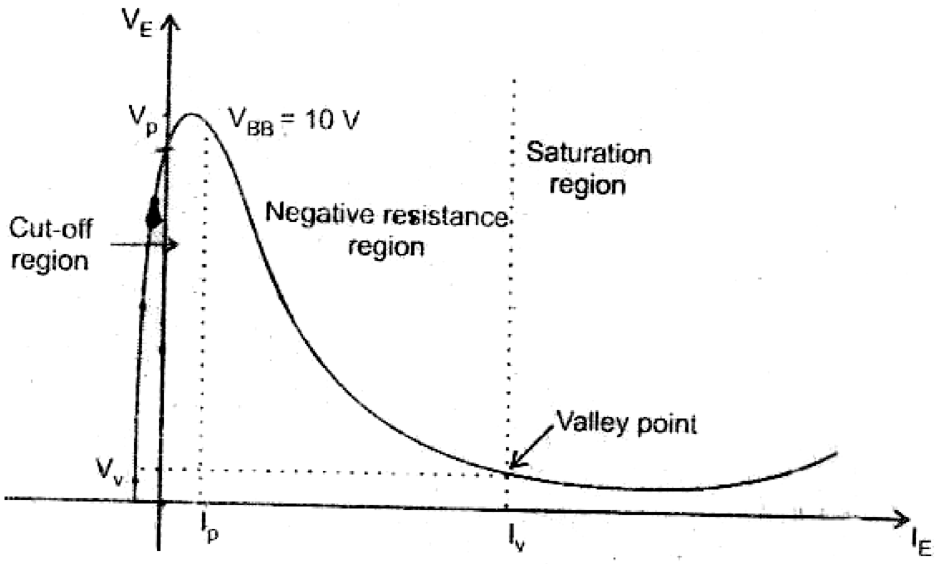


Fig 5.5 UJT CHARACTERISTICS

* Plot between V_E and I_E keeping V_{BB} at constant value.
* When $V_E = 0$, Emitter junction is reverse biased, Emitter current I_{EO} flows.
* Reverse saturation current flows even after increasing V_E upto V_P. This region is known as **"CUT-OFF REGION"**

* When V_E=V_P, diodes start conducting and V_E will decrease with increase in I_E thus establishing a negative resistance region.
* Resistance R_{B1} falls down rapidly and V_E falls to valley voltage V_V.
* Here I_E = I_V(valley current)
* Further increase in I_E causes the device to enter **saturation region.**

5.1.3 UJT AS RELAXATION OSCILLATOR:

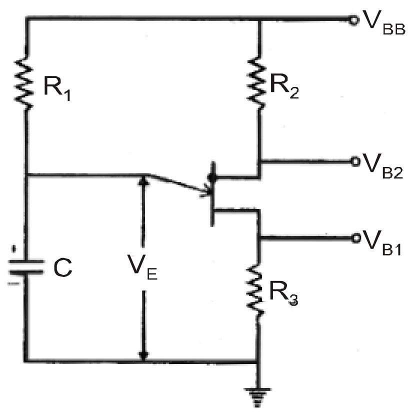


Fig 5.6 UJT as RELAXATION OSCILLATOR

* When V_{BB} is switched ON, Capacitor C charges through R_1.
* When voltage across capacitor is less than V_P, UJT $\rightarrow$OFF condition.
* When voltage across capacitor reaches to V_P, UJT$\rightarrow$turned 'ON' and capacitor discharges through UJT and R_3.
* When voltage across capacitor reaches V_V,C charges through R_1 towards V_P.
* The cycle is repeated continuously generating sawtooth waveform across C.
* Frequency of oscillations of relaxation oscillator,

$$f = \frac{1}{R_T C_T} \ln\left(\frac{1}{1-\eta}\right)$$

5.1.4 FREQUENCY OF RELAXATION OSCILLATOR:

Voltage across capacitor

$$V_C = V_f - (V_f - V_i)\, e^{-t/RC}$$

where V_i = initial voltage across capacitor

V_f= final voltage across capacitor

During charging of capacitor,

$V_i = V_V$; $V_f = V$

at $t = t_1$; $V_C=V_P$

$V_p = V - (V-V_V)\, e^{-t_1/RC}$

$$t_1 = R_1C \ln\left(\frac{V - V_V}{V - V_P}\right)$$

Equation for discharging is

$V_C = V_f - (V_f - V_i)\; e^{-t/RC}$

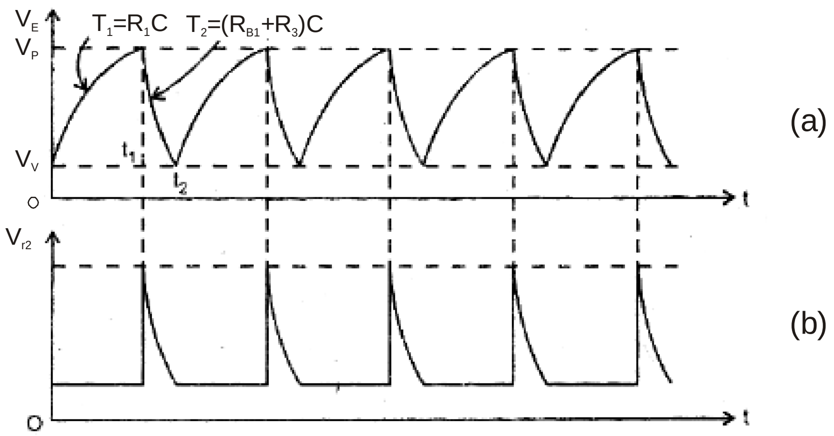


Fig 5.7 (a) The output wave form across capacitor (b) The output waveform across R_2

During discharging $V_f = 0$; $V_i = V_p$

where $R = R_{B1} + R_3$

At $t = t_2$, $V_C = V_V$,

$$V_V = V_P e^{-t_2 (R_{B1}+R_3)C}$$

$$\Rightarrow \boxed{t_2 = (R_{B1} + R_3)C \ln \frac{V_P}{V_V}}$$

Total time period,

$$t_2 << t_1 , T = t_1 + t_2$$

$$T = t_1$$

$$T = R_1 C \ln\left(\frac{V - V_V}{V - V_P}\right)$$

When $V_V << V$

$$T = R_1 C \ln\left(\frac{V}{V - V_P}\right)$$

$$= R_1 C \ln \frac{1}{1 - \frac{V_P}{V}}$$

We know that $V_P = \eta V + V_0$

Neglecting V_0, $V_P = \eta V$

$$\eta = \frac{V_P}{V}$$

$$\therefore T = R_1 C \ln\left(\frac{1}{1-\eta}\right)$$

$$\therefore f = \frac{1}{T}$$

$$f = \frac{-1}{R_1 C \ln\left(\frac{1}{1-\eta}\right)}$$

5.1.5 APPLICATIONS:

* Non sinusoidal oscillator
* Switching circuits
* Timing Circuits
* Voltage regulated supplies

x

5.2 SCR (SILICON CONTROLLED RECTIFIER)

(May / June 2011-16 Marks) (Nov /Dec 2009 - 16Marks) (May/June -2010-8 Marks)(May /June -2014 -16 Marks)

* Silicon Controlled Rectifier $\rightarrow$ 4 layer, 3 junction pnpn device which consists of 3 terminals : **ANODE, CATHODE and GATE**
* 4 layers $\rightarrow P_1, N_1, P_2, N_2$

  3 junctions $\rightarrow J_1, J_2, J_3$

Fig 5.8

a) STRUCTURE OF SCR **b) SYMBOL OF SCR**

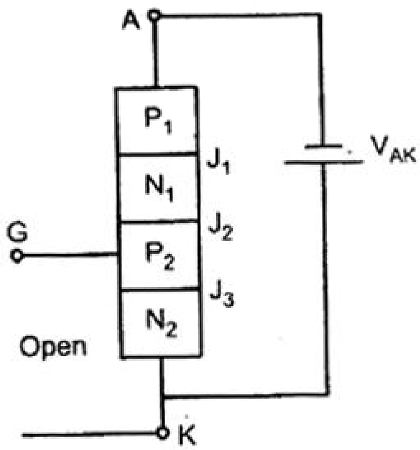
* SCR has 2 states of operation.

* In **OFF State,** it acts as an open circuit between anode and cathode.

* In **ON state,** it acts as a short from anode to cathode.

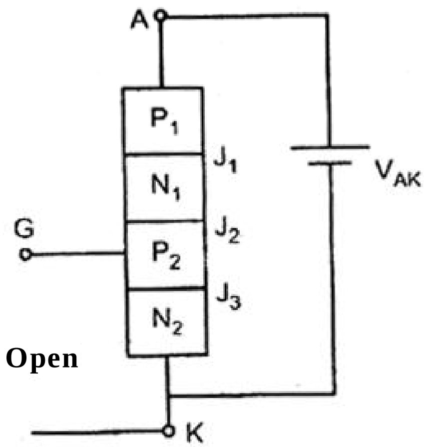
* So SCR behaves like a switch

5.2.1.SCR WORKING:



a) SCR WITH GATE OPEN,

V_{AK} REVERSE BIAS.



B) SCR WITH GATE OPEN

V_{AK} FORWARD BIAS

Fig 5.9

* When anode of SCR is connected to negative terminal of power supply and cathode terminal is connected to positive terminal of power supply, Junctions J_1 and J_3 are reverse biased and junction J_2 is forward biased.

* So SCR is in **TURN OFF CONDITION (Nov/Dec 2009 - 2 Marks)**

* In Fig 5.9 (b), when anode terminal of SCR is connected to positive terminal of power supply and cathode terminal of SCR is connected to negative terminal of power supply, junction J_1 and J_3 are forward biased and junction J_2 is reverse biased.

* So, no current can flow through SCR and SCR is in **CUTOFF.**

* If anode voltage is increased, a stage is reached when junction J_2 is in breakdown and SCR switches to highly conducting state.

* Applied voltage at which SCR starts conducting heavily without gate voltage is called **BREAK OVER VOLTAGE (V_{BO})**

5.2.2 SCR WITH POSITIVE GATE :

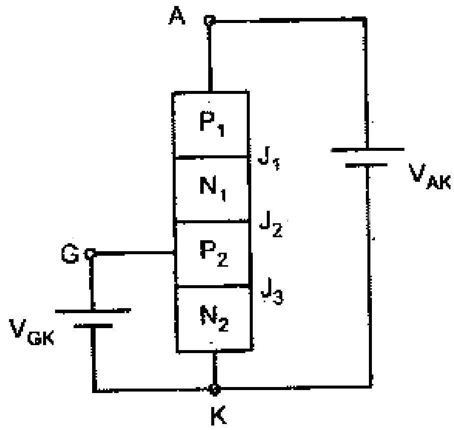


Fig 5.10 SCR with positive gate

* When small positive voltage is applied to gate and anode is connected to positive terminal of supply, junction J_3 is forward biased and junction J_2 is reverse biased.

* Electrons from N_2 layer moves across junction J_3. Similarly holes from P_2 layer crosses junction J_3.

* Gate current flows which increases anode current.

* Increased anode current makes more electrons available at junction J_2.

* The process continues and junction J_2 is in breakdown and SCR starts conducting.

* SCR conducts, even if gate voltage is removed. So SCR cannot be turned OFF.

* However, Anode current can be reduced below the value of holding current I_H to turn OFF SCR.

5.2.3 TWO TRANSISTOR ANALOGY OF SCR :

(May /June 2009 - 10 Marks), (Nov/ Dec -2008 - 2 marks)(Nov/Dec 2010-2 Marks)

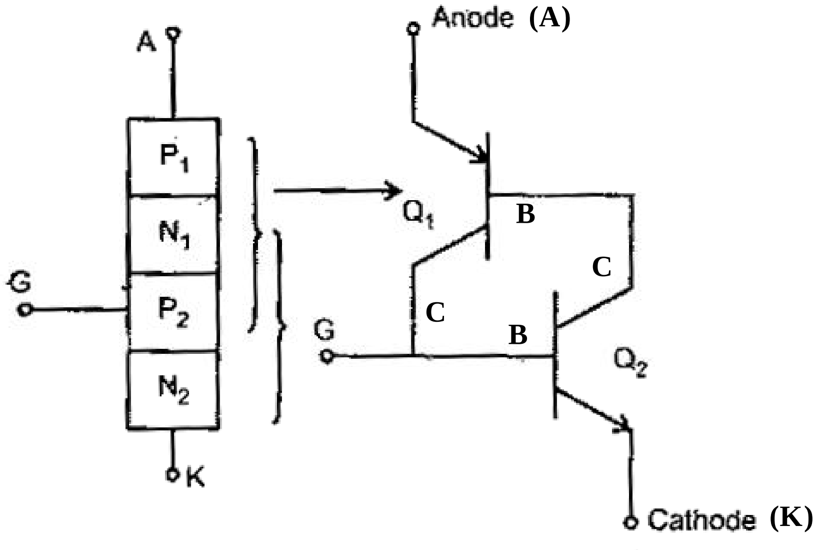


Fig 5.11 Two transistor analogy of SCR

* Upper $P_1N_1P_2$ layer act as transistor Q_1 and layer $N_1P_2N_2$ acts as transistor Q_2.
* Gate terminal is connected to base of transistor Q_2 and collector terminal of Q_1.
* Collector of transistor Q_2 is connected to base of Q_1.
* Therefore, Collector current of Q_2 is equal to base current of Q_1 and base current of Q_2 is equal to collector current of Q_1.
* When applied voltage V_G at gate is 0, Gate current is also zero since tansistor Q_2 and transistor Q_1 are in OFF condition.
* So the current through SCR is '0' and SCR $\rightarrow$ TURN OFF condition.
* When positive pulse of current is applied to Gate and anode terminal is positive w.r.t cathode,then both transistors are turned ON.
* When positive pulse is applied at gate, transistor $Q_1 \rightarrow$ ON and I_{B2} starts flowing and so collector current will increase.

* Collector current of Q_2 = Base current of Q_1,

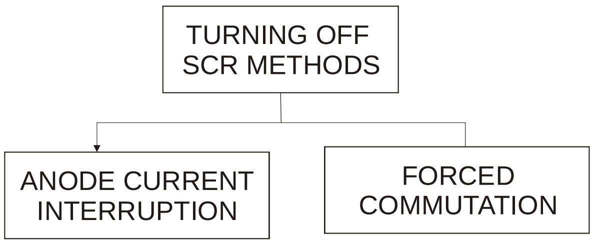
  So collector current of Q_1 increases.

* But Collector current of Q_1= Base current pf Q_2

  Collector current of Q_2 increases.

* Increase of current in one transistor causes increase of current in other transistor.

* Therefore, both transistors Q_1 and Q_2 are driven into saturation and SCR is in TURN ON condition.



(Anode current is reduced to ‘0’ or reduced to a value less than holding current (I_H))

(Current through SCR is forced to change its direction opposite to forward conduction such that the net forward current is reduced below holding value)

5.2.4 SCR CHARACTERISTICS :(Nov /Dec 2010 - 2Marks)

A) FORWARD CHARACTERISTICS:

* When anode is positive w.r.t. cathode, curve between applied voltage and SCR current is called **"FORWARD CHARACTERISTICS"**

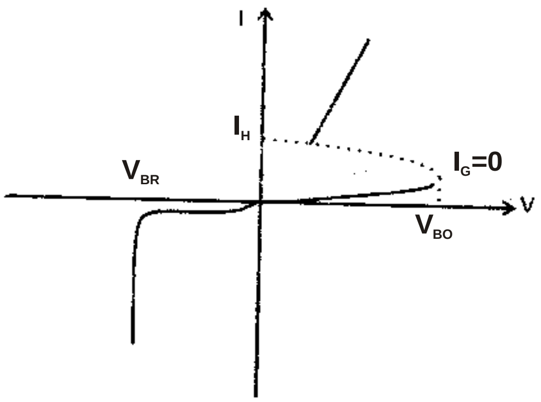
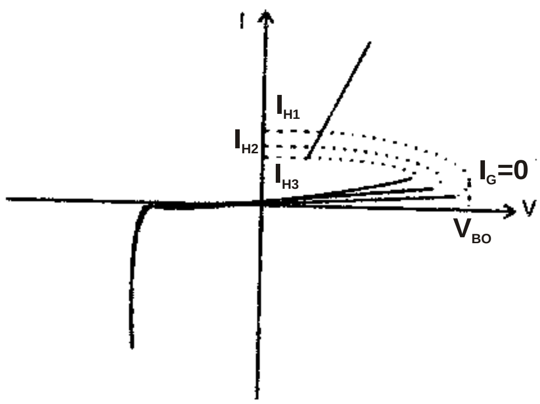


Fig.5.12 (a) Characteristics of SCR



(b) SCR Characteristics for Different Values of I_G

* Current through SCR is '0' until the applied voltage is less than breakover voltage of SCR.

* When applied voltage is slightly greater than V_{BO}, SCR starts conducting heavily.

* In this condition, voltage across SCR drops suddenly. This is shown in fig 5.12 (a).

* In Fig 5.12(b), When I_G is increased, SCR turns ON at very low anode - to - cathode voltage.
* Gate current controls required anode - to - cathode voltage to turn ON SCR. Corresponding voltage is known as **Breakover voltage.**
* Breakover voltage required to turn '**ON**' SCR decreases as gate current increases.

B) REVERSE CHARACTERISTICS:

* When anode is negative w.r.t cathode, curve between V and I is known as **REVERSE CHARACTERISTICS.**
* When reverse voltage is applied to SCR, current through SCR is very small. This current is called as **LEAKAGE CURRENT.**
* When reverse voltage is increased gradually, a stage is reached at which the avalanche breakdown occurs and SCR conducts heavily in reverse direction.
* Maximum reverse voltage at which SCR conducts heavily in reverse direction is known as "**REVERSE BREAKDOWN VOLTAGE**".

5.2.5 IMPORTANT DEFINITIONS ASSOCIATED WITH SCR:

1. BREAK OVER VOLTAGE (V_{BO}):

→ Voltage at which SCR enters conduction region.

2. HOLDING CURRENT (I_H):

→ Value of anode current below which SCR switches from ON state to OFF state.

3. GATE TRIGGER CURRENT (I_{GT}):

→ Value of gate current necessary to switch SCR from OFF state to ON state.

4. FORWARD CONDUCTION REGION:

→ Region corresponds to ON condition of SCR

5. FORWARD BLOCKING REGION:

→ Region corresponds to OFF condition of SCR when anode is positive w.r.t cathode.

6. REVERSE BLOCKING REGION:

→ Region corresponds to OFF condition of SCR when anode is negative w.r.t cathode.

7. REVERSE BREAKDOWN VOLTAGE:

→ Value of reverse voltage from cathode to anode at which the device breaks into avalanche region and begins to conduct heavily.

5.2.6 APPLICATIONS OF SCR:

→ Relay control

→ Half wave power control

→ Motor control

→ Phase control

→ Regulated power supplies

x

5.3 DIAC (DIODE A.C. SWITCH) (Nov /Dec 2010 - 5 Marks) (Nov/Dec 2008 - 8 Marks) (May / June 2012 - 8 Marks) (Nov/Dec -2012 - 8 Marks)

→ 5 layer device

→ Triggers Triacs and provides protection against high voltages

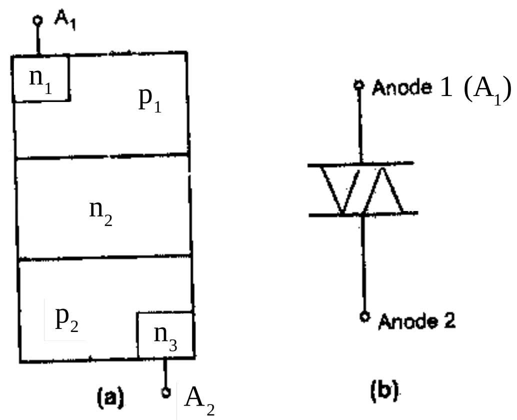


Fig 5.13 (a) DIAC CONSTRUCTION (b) DIAC SYMBOL

* DIAC has 2 terminals named anode 1 (A_1) and anode 2 (A_2). There is no cathode.

* But each terminal can serve as anode or cathode depending on polarity of applied voltage.

* If terminal voltage at anode 1 is positive w.r.t. anode 2 and greater than V_{BO}, P_2 region serves as anode.

* Similarly, Negative voltage at anode 2 terminal pulls holes from P_1 region towards the terminal and pushes electrons from n-region across junction into P_1 region making them available for conducting.

* Current flow path is P_2- N_2-P_1-N_1.

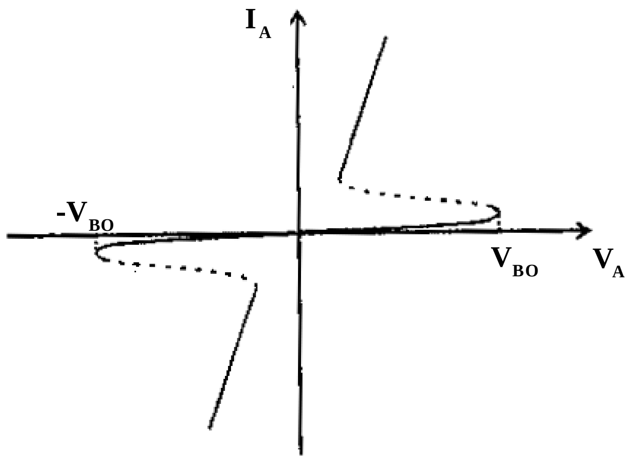


Fig 5.14 DIAC CHARACTERISTICS

* When voltage at terminal A_2 is positive w.r.t. A_1 and greater than V_{BO}, Current path is P_1 - N_2 - P_2 - N_3.
* DIAC remains nonconducting until applied voltage is less than breakdown voltage.
* When applied voltage is greater than breakdown voltage, DIAC turns ON and remains ON until applied voltage is reduced below holding value.

APPLICATIONS:

→ Power Control

→ Motor Speed Control

→ Proximity detector

→ Triggering TRIAC.

X

5.4 TRIAC (TRIODE A.C. SWITCH) (Nov/Dec 2008 - 8 Marks)(Nov /Dec 2010 - 5 Marks) (May /June 2009 - 6 Marks) (May /June 2010 - 8 Marks)

→ 3 terminal, 5 layer, bi directional device.

→ Consists of three terminals anode 1 (A_1), anode 2 (A_2) and Gate (G).

→ Acts like two SCR's in parallel with common gate terminal.

→ P_2, N_1, P_1, N_4 →forms one SCR.

→ P_1, N_1, P_2, N_2 forms another SCR.

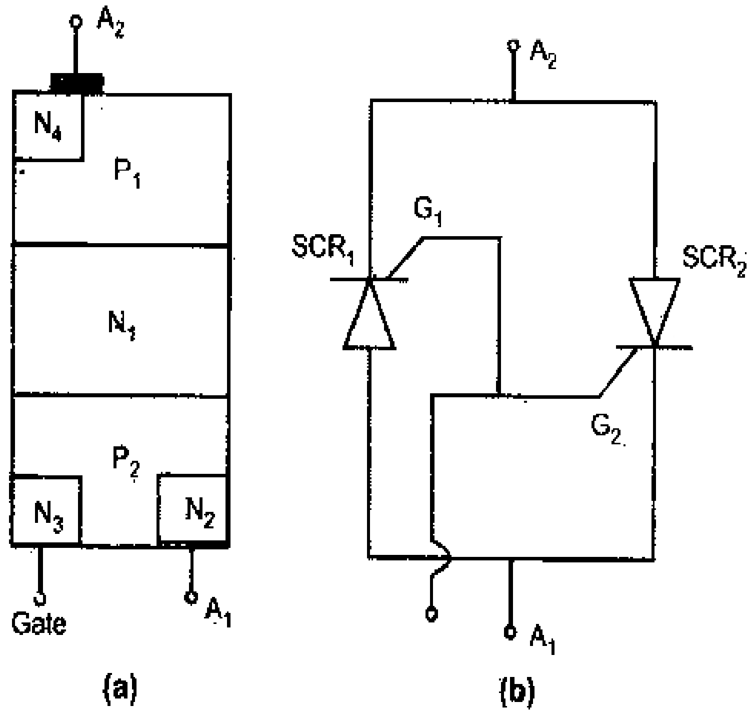
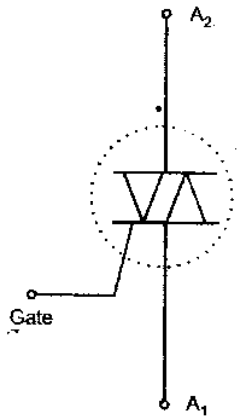


Fig 5.15 (a) TRIAC - CONSTRUCTION (b) TWO - SCR EQUIVALENT



(c) TRIAC - SYMBOL (May /June - 2014 - 2 Marks)

* In Fig 5.15(b), cathode of SCR_1 is connected to anode of SCR_2 and cathode of SCR_2 is connected to anode of SCR_1.
* Gates of both SCR's are connected to common terminal.
* TRIAC conducts in either direction.
* Characteristics of Triac are same as forward biased SCR.
* TRIAC allows current flow in both directions. So it is called **BI - DIRECTIONAL DEVICE.**

5.4.1. WORKING OF TRIAC:

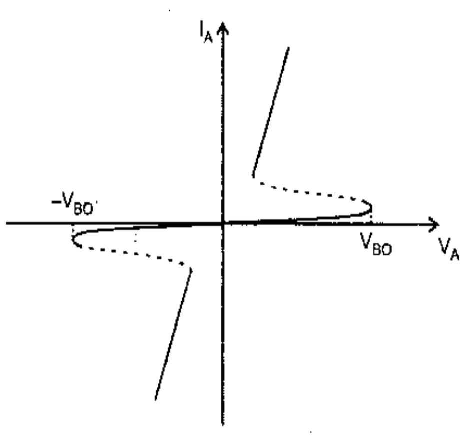


Fig 5.16 Triac Characteristics (May/June 2011 - 2 Marks)

* When terminal A_1 is positive w.r.t. A_2 and gate is either negative or positive.(with

SCR 'ON'), Current flow is from P_2,N_1, P_1,N_4.

* So, the junctions P_2, N_1 is reverse biased.

* When terminal A_2 is positive w.r.t. A_1 and gate is either positive or negative (SCR_2 is ON), Current flow is from P_1, N_1, P_2 to N_2.

* So, the junctions P_1-N_1 and P_2 - N_2 are forward biased and N_1 - P_2 junction is reverse biased.

5.4.2 ADVANTAGES:

* Can be turned 'ON' by pulse of gate current and does not require breakdown voltage to initiate conduction.

* Stops conducting when anode current drops below specified value of holding current (I_H).

5.4.3 APPLICATIONS:

* Heater Control

* Motor Speed Control

* Light dimming control

* Phase control

X

5.5 LED (LIGHT EMITTING DIODE) (Nov / Dec 2012- 8 Marks) (Nov/Dec -2010- 6 Marks)(Nov /Dec 2009 - 5 Marks)

→ Light Emitting diode, commonly known as LED → diode which gives unstable light when it is energized.

→ Works on the principle of **Electroluminescence.**

→ **ELECTROLUMINESCENCE** →Process that changes electrical input to light output (opposite of PHOTOVOLTAIC EFFECT)

5.5.1 CLASSIFICATION OF LEDS:

1) SURFACE EMITTING LEDs

2) EDGE EMITTING LEDs

* In **Surface Emitting** structure, light radiates perpendicular to plane of pn junction.

* In **Edge emitting** LEDs, light is confined to a plane and radiates parallel to junction.

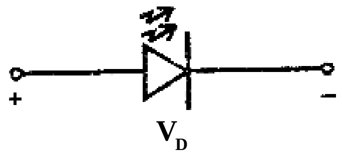


Fig 5.17 Symbol of LED

* When diode is **FORWARD BIASED**, free electrons from n-side and holes from p-side move towards the junction.

* Electrons from n-side cross the junction and fall into holes. So, **RECOMBINATION** takes place.

* Since Electrons fall from high energy level to low energy level during recombination, it radiates energy.

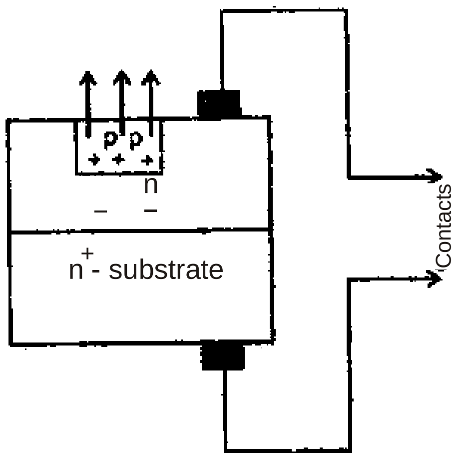


Fig 5.18 SURFACE EMITTING LED

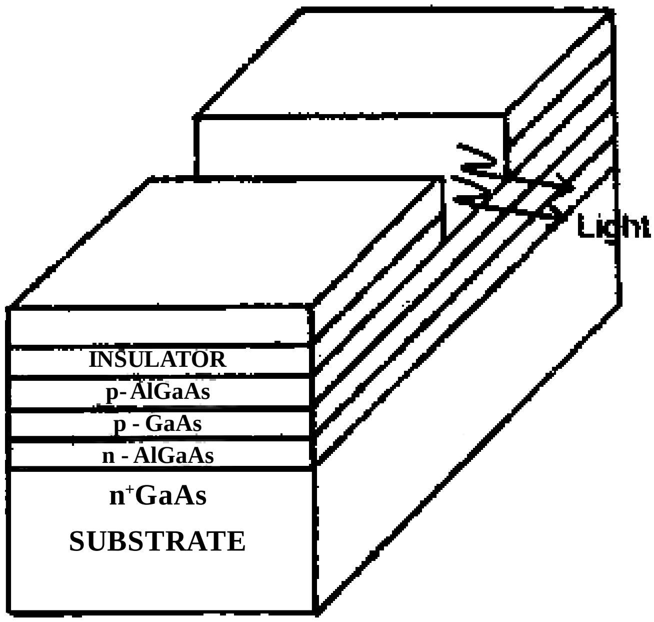


Fig 5.19 EDGE EMITTING DIODE

* If diode →Silicon or Germanium, energy goes off in form of **heat**.

* If diode →GasAsP (Gallium Arsenide Phosphide) or GaP(Gallium Phosphide), energy radiates as **light.**

* Colour of light emitted by LED depends on wavelength of light.

COMPONENT	WAVELENGTH	COLOUR
GaP	565	GREEN
GaAsP	590	YELLOW
GaAsP	632	ORANGE
GaAsP	649	RED
GaAlAs	850	Near IR
GaAs	940	Near IR

5.5.2 LED - CHARACTERISTICS :

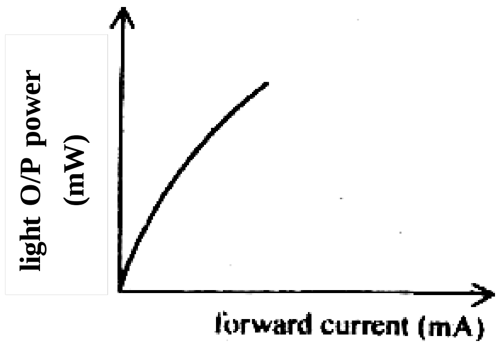


Fig 5.20 LED CHARACTERISTICS

* Amount of light emitted is proportional to forward current.

* When forward current is high, light output is high.

5.5.3 ADVANTAGES

* Small in size
* Low cost
* Long life time
* Control of Intensity is easy

5.5.4 APPLICATIONS

→ Numeric display in pocket calculators.

→ Burglar - alarm system

→ Used in image sensing circuits

→ Used for solid video displays

1. SPECIFIC APPLICATIONS - SEVEN SEGMENT DISPLAY :

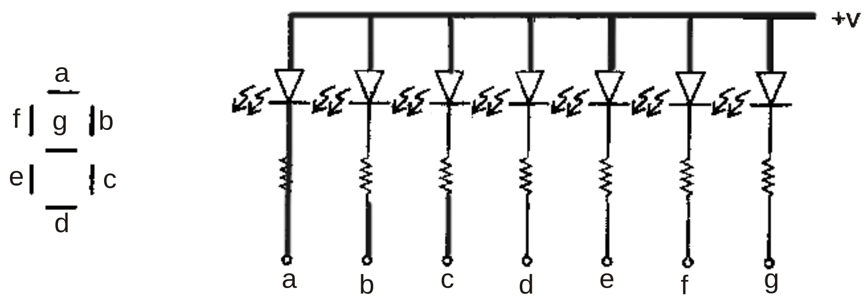


Fig 5.21

* It is called as COMMON ANODE FORM since all anodes are connected to common point.

* If positive voltage is connected to common anode w.r.t. ground, each individual segment is activated.

2. SPECIFIC APPLICATIONS – INFRARED EMITTERS

→ **Solid state** Gallium Arsenide devices which emit beam of light when forward biased.

→ Consists of a pn junction. When junction is forward biased, electrons from n-region recombine with excess holes in p- region.

→ During recombination, energy is radiated in the form of **photons**.

→ Radiant energy →**INFRARED REGION**

Used in

* Shaft encoders
* Intrusion alarms
* Paper - tap readers

x

5.6 DIFFERENCES BETWEEN SCR AND TRIAC

SCR	TRIAC
* Unidirectional device	* Bidirectional device

* Fast turn OFF time,therefore used as a switch.	* Slow turn OFF time
* Triggered by UJT	* Triggered by DIAC
* **APPLICATIONS:** Phase Control, Protection of Power supplies, etc..,	* **APPLICATIONS:** Light dimmer, Motor control

x

5.7 LCD (LIQUID CRYSTAL DISPLAY)(Nov /Dec 2010 - 6 Marks) (May /June 2009- 16 Marks) (May /June 2012 - 8 Marks)

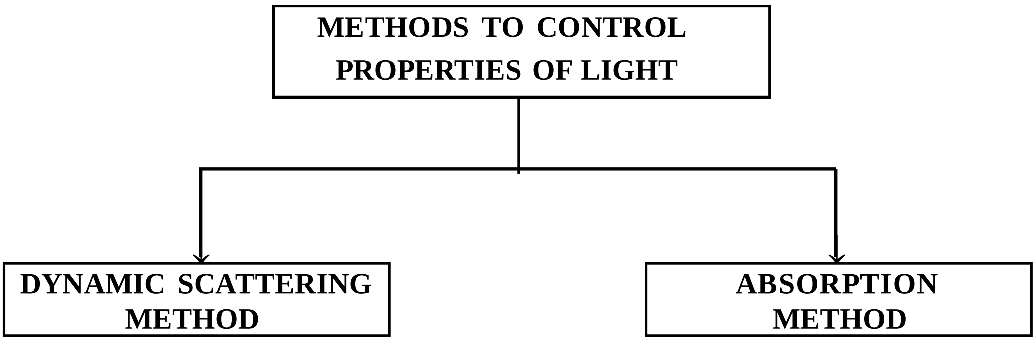
→ Electronic display device which operates by applying varying electric voltage to a layer of liquid crystal which induces changes in its optical properties.

→ Passive type display device which displays alpha numeric characters.

5.7.1 STATES OF MATTER:

* Solid, liquid, Gas and Liquid crystal
* **Liquid crystal phase** exists between solid and liquid phase.
* The molecules maintain their orientation like molecules in solid but also move around to different positions like molecules in liquid.

5.7.2 METHODS TO CONTROL LIGHT PROPERTIES:



1) DYNAMIC SCATTERING METHOD:

* When electric potential is applied, molecules in liquid crystal acquire random orientation.
* Light passing through the material is reflected in many directions.

2) ABSORPTION METHOD:

* Molecules are oriented in such a way that they alter polarization of light passing through the material.

* Polarizing filters absorbs or passes the light.

5.7.3 OPERATION MODES :

MODES OF OPERATION

TRANSMISSIVE MODE
(Light passes completely through LCD and is altered as it passes through liquid crystal)

REFLECTIVE MODE
(Light passes through the material when it is altered and reflected by mirror to emerge from the same side it entered)

5.7.4 CONSTRUCTION OF LCD:

* Composed of multiple layers
* A sheet of glass is coated with transparent metal oxide film which acts as electrode.
* Electrodes sets voltage across the cell necessary for orientation transition.
* Electrodes are etched in patterns or individually accessible segments which are energized to create desired display.

5.7.5 BASIC MODES:

1) Dynamic Scattering LCD - Transmissive mode
2) Dynamic Scattering LCD - Reflective mode
3) Absorption mode LCD - Transmissive mode
4) Absorption mode LCD - Reflective mode

1) DYNAMIC SCATTERING LCD - TRANSMISSIVE MODE

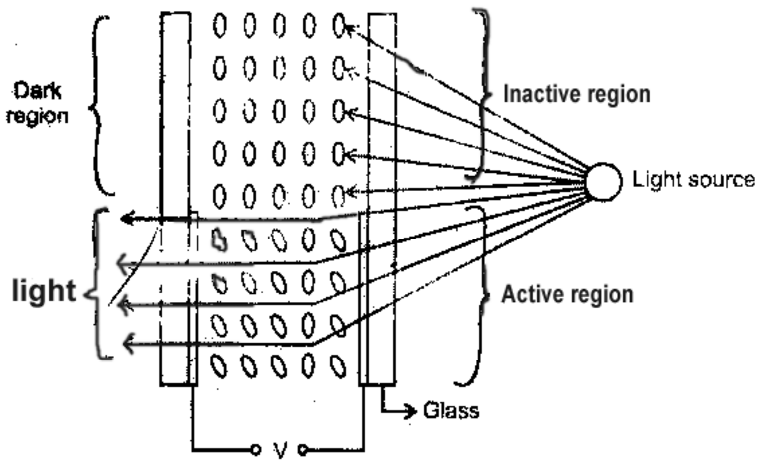


Fig 5.22 Dynamic scattering LCD - transmissive mode

* Under external electric field, molecules have random orientation.
* Molecules in **inactive region** have **definite** alignment.
* In **Active region**, due to **random** orientation of molecules, light will be scattered and escape with **bright appearance**.

2) DYNAMIC SCATTERING LCD - REFLECTIVE MODE

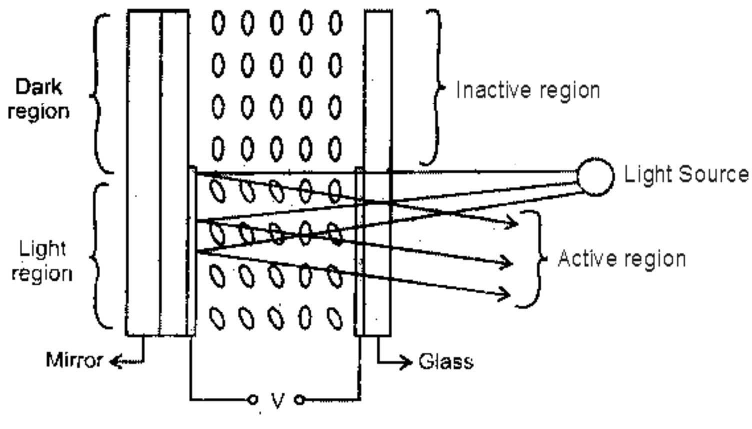


Fig 5.23 DYNAMIC SCATTERING LCD - REFLECTIVE MODE

* Same as that of transmissive mode except that mirrored surface is replaced or added behind one of the glass sheets.
* But, unwanted reflections limit **readability** of display of this mode.

3. ABSORPTION MODE LCD - TRANSMISSIVE MODE:

* Light enters Twisted Nematic crystal cell through vertical polarizer.
* When applied potential is zero due to molecular twist, vertically polarized light becomes horizontally polarized light and absorbed by vertical polarizer at other end.

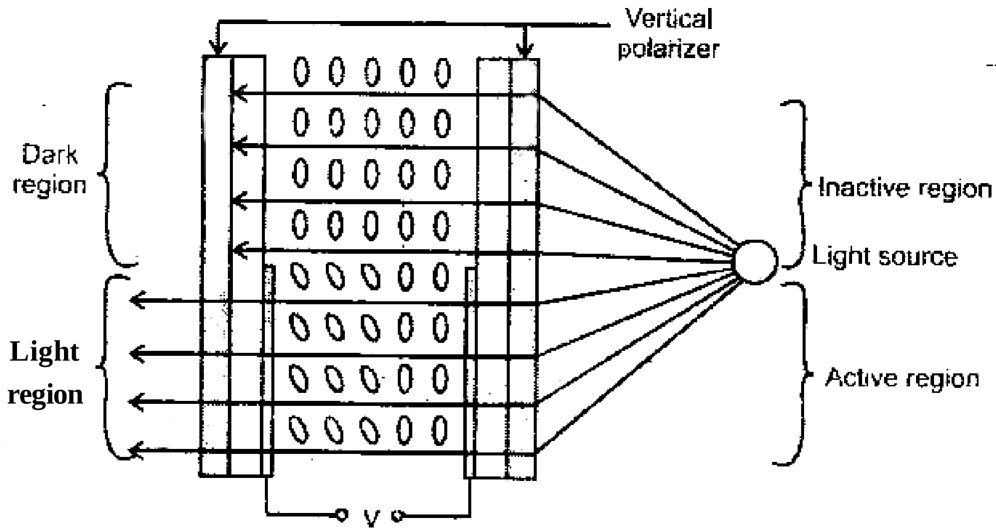


Fig 5.24 ABSORPTION MODE LCD - TRANSMISSIVE MODE

* **Inactive Region** appears **dark.**
* **In Active Region**, there is no change in polarization. So vertically polarized light which enters cell, leaves the cell without any change and is not absorbed by vertical polarizer.
* So **Active Region** appears **bright**.

4) ABSORPTION MODE LCD - REFLECTIVE MODE

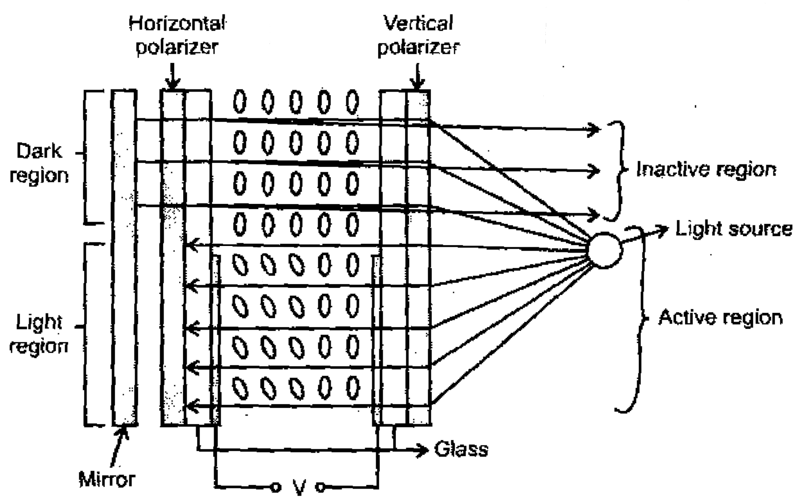


Fig 5.25 ABSORPTION MODE LCD - REFLECTIVE MODE

* Mirror is used behind Horizontal polarizer.
* Horizontal polarizer is placed between one of the glass sheets and mirror.
* Vertical polarized light enters inactive region and becomes horizontal polarized.
* Light passes through horizontal polarized light and **deflected** back due to **mirror**.
* Unsaturated region shifts horizontal polarized light to vertical polarized light.
* So, **Reactivated** region appears **bright**.
* In **Active region**, vertical polarized light does not undergo any changes and absorbed by horizontal polarized light. So the region appears dark.

5.7.6 ADVANTAGES OF LCD:

* Economical
* Low power consumption
* Good range of colour choice

5.7.7 DISADVANTAGES OF LCD:

→ Response time is below 100-300 ms.

→ Life time is less when used with Direct current.

→ Occupies large area.

5.7.8 APPLICATIONS:

* Calculators
* Watches
* Higher end CRO's
* Laptop Computers

LED	LCD (May/June 2011-2 Marks)
* More life time	* Life time limited to 10,000 hours.
* Consumes more power	* Consumes less power
* External circuitry is required when driven from IC's	* Can be driven directly from IC's
* High response time (100 ns)	* Less response time (100-300 ms)

X

5.8 PHOTO TRANSISTOR (Nov/Dec 2010 - 5 Marks) (Nov /Dec 2009 - 5 Marks)

* 2 lead or 3 lead device.
* In 2 - lead photo transistor, base terminal does not exist. Light intensity is applied as input to transistor.
* In 3 - lead phototransistor, base terminal is provided so that the device can be used as ordinary BJT.

* **PHOTO TRANSITOR** → Light detector.

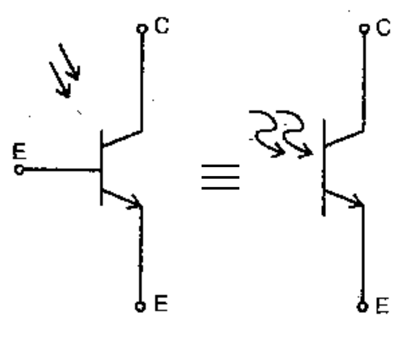


Fig 5.26 (a) SYMBOL OF PHOTOTRANSISTOR

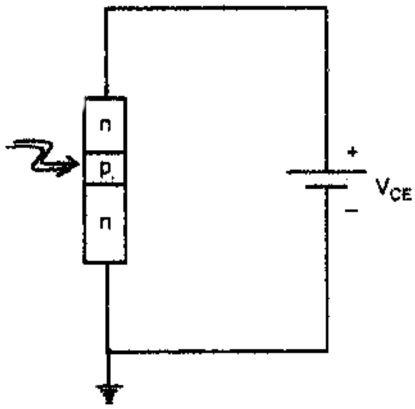


Fig 5.26 (b) PHOTOTRANSISTOR

* Consider an ordinary transistor in CE configuration with Base terminal Open circuited.
* Assume that there is no illumination.

Collector current $I_C = \beta_{dc} I_B + (1 + \beta dc) I_{CBO}$

Base current $I_B = 0$

$\therefore I_C = (1 + \beta dc) I_{CBO}$

$$\boxed{I_C \approx \beta_{dc} I_{CBO}}$$

* Collector current depends on Collector base leakage current which is due to thermally generated minority carriers.
* When light energy is incident on Collector - base junction, additional minority carriers are generated.
* If $I_L \rightarrow$ Current due to additional minority carriers.

$$\boxed{I_C = \beta_{dc}\left(I_{CBO} + I_L\right)}$$

5.8.1 V- I CHARACTERISTICS:

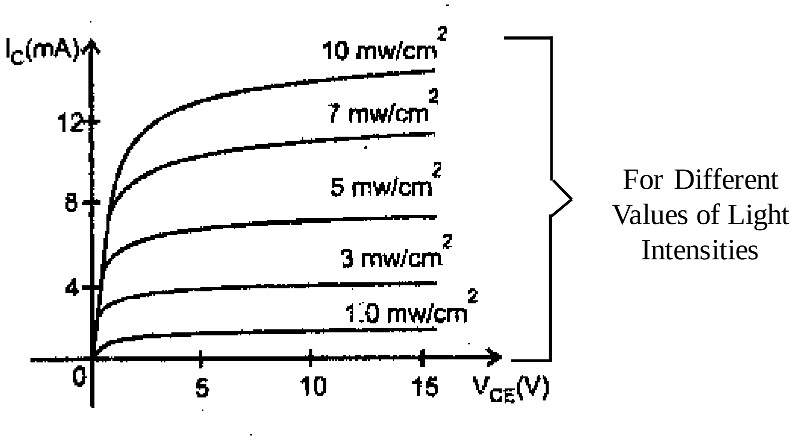


Fig 5.27 V- I CHARCTERISTICS

- Plot between Collector to Emitter voltage (V_{CE}) and Collector current (I_C)for different values of light intensities.
- Characteristic curves are similar to output characteristics of CE transistor.
- Increase in light intensity corresponds to increase in collector current.
- For given light intensity, phototransistor produce greater output current than photo diode.

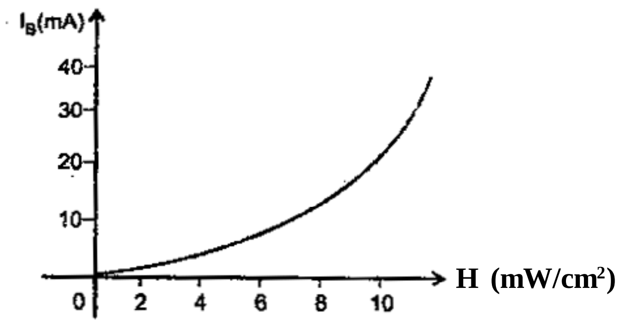


Fig 5.28 RADIATION FLUX H (mW/cm²)CHARACTERISTICS OF PHOTOTRANSITOR

5.8.2 APPLICATIONS:

* Alarm systems
* Lighting control
* Punch - Card Reader
* Light operated Relay Circuits.

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5.9 SOLAR CELLS

(May /June 2010 - 2 Marks, Nov /Dec 2012 - 8 Marks, Nov /Dec 2010 - 2 Marks, May/June 2012 - 8 Marks, May/June 2014 - 8 Marks)

* **Solar Cell** → pn junction device with no voltage applied directly across junction.
* Solar Cell → Converts photon power to electrical power and delivers the power to load.
* It is a device which converts sunlight directly into electricity.
* Made of semiconductor material such as Silicon, Selenium, Gallium Arsenide, Indium Arsenide.
* The Semiconductor material absorbs solar protons and converts energy into electric current.
* Process of converting light energy to electric energy →**PHOTOVOLTAIC EFFECT**

5.9.1 SYMBOL AND CONSTRUCTION OF SOLAR CELL

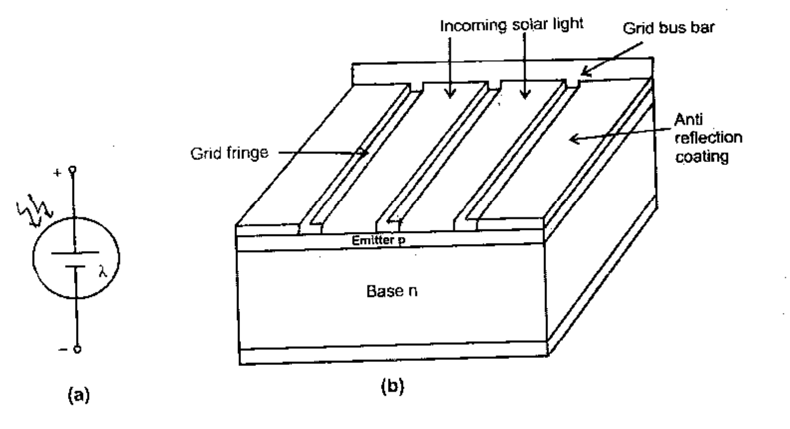


Fig 5.29 (a) SYMBOL OF SOLAR CELL (b) CONSTRUCTION OF SOLAR CELL

* Consists of 2 layers doped with n-type and p-type material.
* The 2 layers form pn junction,

  Thicker layer $\rightarrow$ BASE LAYER

  Thinner layer $\rightarrow$ EMITTER LAYER
* Base layer $\rightarrow$ n-type

  Emitter layer $\rightarrow$ p - type
* Solar cell has p on n polarity.
* When light energy falls on solar cell, it collides with valence electron and gives sufficient energy to leave parent atom. This creates hole in valence band.
* So, free electrons and holes are generated on each side of the junction.
* Minority electrons which are generated in p- type will move freely across the junction and holes generated in n-type material also move towards the junction.
* Minority carriers are **swept** over the junction if their diffusion lengths are very large.
* Current due to minority carrier flow $\rightarrow$ **PHOTO CURRENT.**
* Direction of current is opposite to direction of conventional forward current of p-n junction.

5.9.2 SOLAR CELL CHARACTERISTICS:

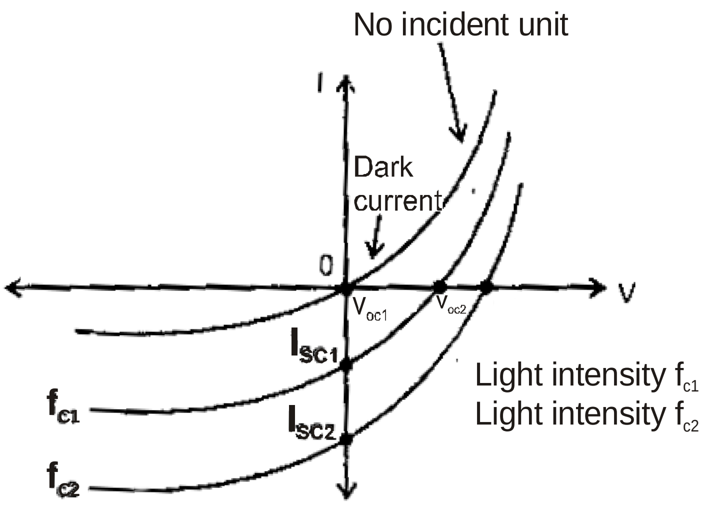


Fig 5.30 I_{SC} and V_{DC} Versus light intensity

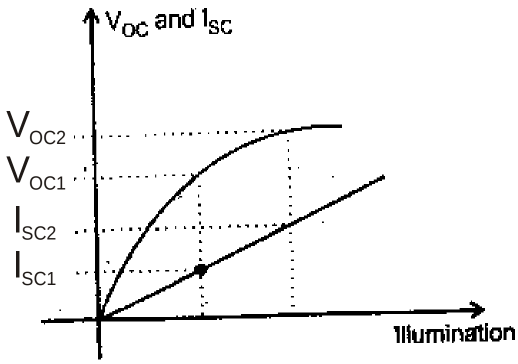


Fig 5.31 V_{OC} & I_{SC} Vs ILLUMINATION

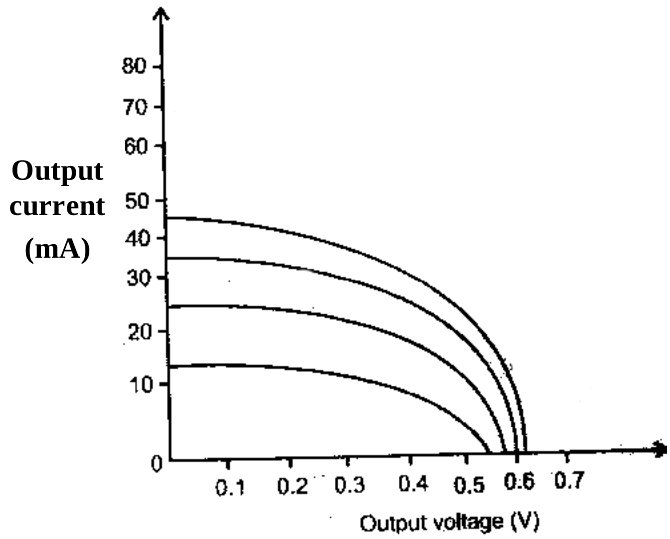


Fig 5.32 Output Characteristics of a solar cell

5.9.3 APPLICATION:

* Space Crafts
* Voltage Regulators across load.

x

5.10 OPTO COUPLER (May /June 2014 -2 Marks)

* **Opto Coupler** or **Opto Isolator**→provides complete electric isolation between electronic circuits.
* Isolation is needed to provide protection from high voltage transients which may damage the device.
* Consists of 2 main components - **Optical transmitter** (LED or infrared LED) and **Optical Receiver** (Photo transistor)

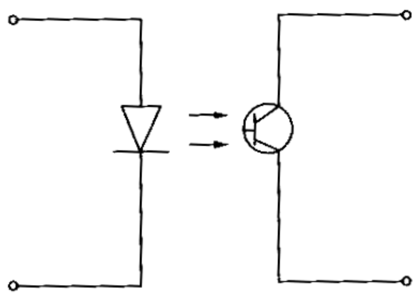


Fig 5.33 OPTO COUPLER

* The 2 components are separated by transparent barrier which does not allow passage of light.
* **CONFIGURATION :** 6-pin or 8 - pin package.
* Package structure permits electrical signal in one way (from LED to photo detector)
* Provides **high isolation resistance ($10^{11}\Omega$) and high isolation voltages (500V-2500V)**
* Light intensity of input LED depends on variation in input signal.
* Light intensity, when applied to photo transistor, turns 'ON' phototransistor and produces current through external load.

PARAMETERS:

1. TRANSFER GAIN:

$$\text{Transfer gain} = \frac{\text{Output voltage}}{\text{Input current}}$$

2. ISOLATION VOLTAGE:

→ Maximum voltage existing between input and output terminals without occurrence of dielectric breakdown.

3. DC CURRENT TRANSFER RATIO (%):

$$\text{DC current transfer Ratio} = \frac{\text{Output current}}{\text{Input current}}$$

x

5.11 CHARGE COUPLED DEVICE (CCD) (Nov/Dec -2009 - 6 Marks) (May /June 2014 - 8 Marks)

* CCD → Integrated circuit etched onto Silicon surface forming light sensitive elements called "**PIXELS**"
* Photons incident on this surface generate charges which can be read and turned into digital copy of light patterns falling on the device.
* CCD → 3 layer structure
* Consists of uniformly doped semiconductor substrate over which thin layer of SiO_2 is deposited.
* SiO_2 layer→ insulator
* On top of SiO_2 layer is an array of closely spaced metal electrodes which are connected to negative potential with respect to substrate.
* The potential induces holes in substrate forming depletion layer.
* Depth of depletion layer depends on magnitude of potential applied.

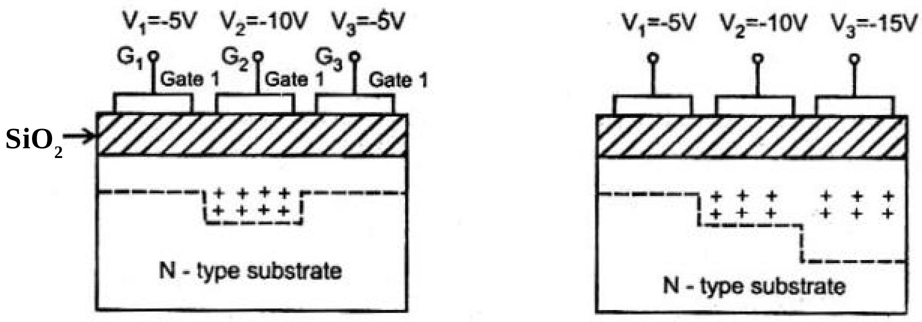


Fig 5.34 (a) Charge Storage Condition (b) Charge Transfer Condition

* If potential V_2 (-10V) is greater than V_1 is applied to gate 2, minority carriers under gate 1 transfers to region under gate 2.

* If potential applied to gate 3 is less than that of gate 2, then charge transfer does not occur and charge is stored below G_2. This is known as **CHARGE STORAGE CONDITION**
* If applied potential (V_3) to gate 3 is greater than V_2, minority charge under gate 2 transfers to region under gate 3. This is known as **CHARGE TRANSFER CONDITION.**

APPLICATIONS:

* Photo Sensor arrays
* Solid State images (Video Camera)
* Memory and image sensors
* Dynamic Shift Registers in Computers.

X

5.12 POWER - BJT, POWER MOSFET, D - MOS AND V - MOS

5.12.1 INTRODUCTION:

* Output stages of most amplifiers consist of **Power stage.**
* They require power conversion (DC - DC conversion)
* So, Power Converters are needed for long operating times and low power consumption.
* **Example :** Diode, SCR, DIAC, TRIAC, BJT, MOSFET

5.12.2 POWER BJT:

* Modified version of small signal BJT.
* Lightly doped (N^-) material is introduced between base and collector region.
* Due to introduction of N^- layer, reverse biased voltage increases.
* Amplification factor and Breakdown voltage depends on Base Width.
* Base Width is kept larger than small signal BJT.

When $I_B = 0$, Collector current will be negligible

$$I_C \approx I_{CBO}$$
$$V_{CE}\,(sat) = V_{CC}$$

When $V_{BE} > 0.7V_{DC}$, I_C gradually increases

$$I_C \approx \beta I_B$$
$$V_{CE(sat)} = 0.2V$$

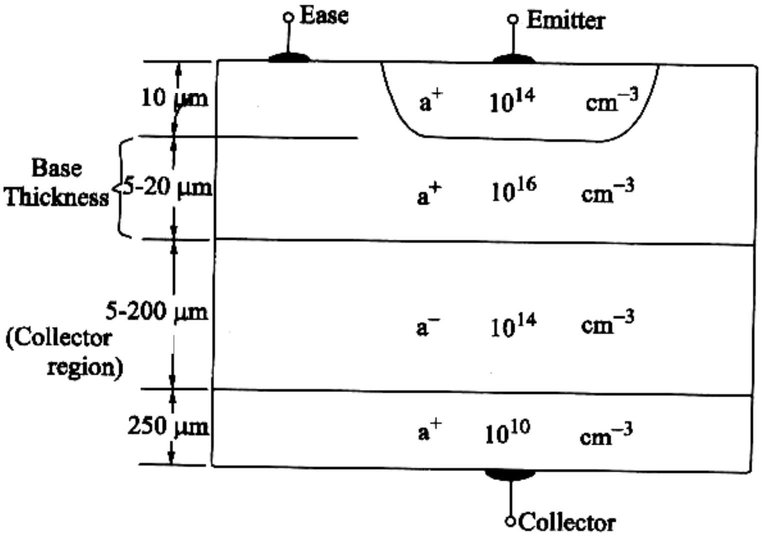


Fig 5.35 POWER BJT

ADVANTAGES:

* Current crowding is avoided.
* Decreases Power dissipation
* Decrease ON state resistance
* Minimizes thermal resistance

5.12.3 POWER MOSFET

* Similar to Bipolar transistor
* POWER MOSFET → Voltage controlled device
* Bipolar transistor →Current controlled device
* Large base drive current which is high as one fifth of collector current keeps device in ON state.
* Higher reverse base drive currents are required to obtain fast turn - off.

5.12.4 DISADVANTAGES OF BJT & ADVANTAGES OF POWER MOSFET:

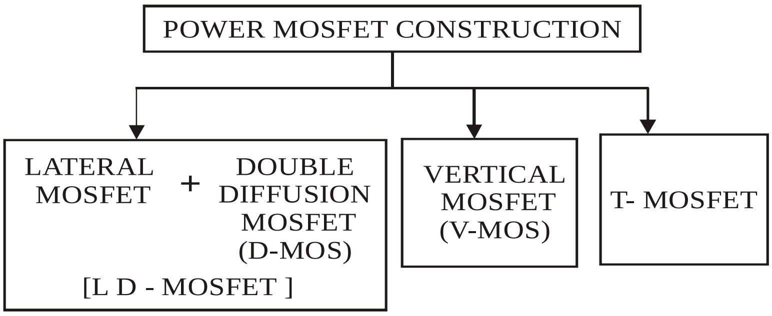
(A) BJT DISADVANTAGES:

→ Electrons and holes contribute to conduction.

→ Presence of holes with higher carrier lifetime causes low switching speed.

B) POWER MOSFET ADVANTAGES:

* High input impedance.
* Do not suffer from minority carrier storage time effects.
* Do not suffer from thermal runaway and breakdown.



1) a) LATERAL MOSFET

* Working of lateral MOSFET is similar to small signal MOSFET.
* Because of blocking PN junction, no current can flow with no electrical bias applied to gate G.

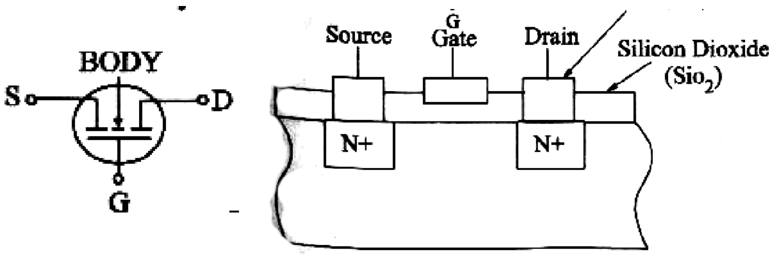
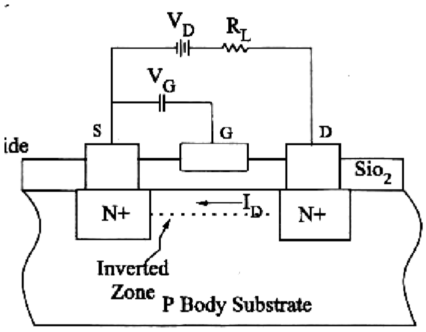


Fig 5.36 (a) SYMBOL (b) LATERAL MOSFET



(c) CIRCUIT CONNECTIONS IN LATERAL MOSFET

* When V_{GS} and V_{DS} is applied, free hole carriers in p- epitaxial layer are repelled away from gate area creating a channel which allows electron to flow from source to drain.
* Lateral MOSFET is operated in Enhancement mode.

A) ADVANTAGES:

* Low gate signal power requirement.
* Fast switching speeds because electrons can flow from drain to source when channel opens.

B) DISADVANTAGES:

→ Channel length cannot be made shorter to support rated voltage.

→ Setting up wider channels is costly.

1.b) DOUBLE DIFFUSION MOSFET (D-MOS)

→ Current path is created by inverting p-layer underneath the gate.

→ Source current flows underneath the gate area and flows vertically through drain and then spreads out.

→ Consists of thousand of N+ sources conducting in parallel directions.

→ Responsible for low ON - state resistances [R_{DS}(ON)] for same blocking voltage and faster switching.

→ $$R_{DS(ON)} = R_{SOURCE} + R_{CH} + R_{A} + R_{J} + R_{D} + R_{SUB}$$

where R_{SOURCE} = Source diffusion resistance

R_{CH} = Channel Resistance

R_{A} = Accumulation resistance

R_{J} = JFET component resistance of region between 2 body regions.

R_{D} = Drift region resistance

R_{SUB} = Substrate resistance

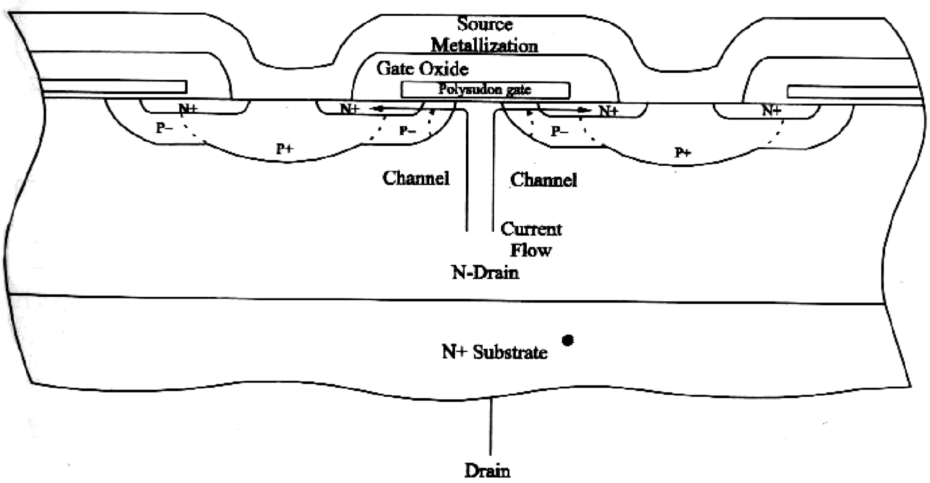


Fig 5.37 D-MOS

A) ADVANTAGES:

* Low gate signal power requirement
* Fast switching speeds because electron can flow from drain to source when channel opens.

B) DISADVANTAGES:

* Channel length cannot be made shorter to support rated voltage of device.
* Setting up wider channels is costly.

1.C) LATERAL DOUBLE DIFFUSION MOSFETS (LD MOSFET)

→ Low ON resistance and high blocking voltage.

→ Channel width is lower than E-MOSFET

→ Used in RF power amplifier, UHF, Power Amplifier in broadcast and radar system.

2) VERTICAL MOSFET (V-MOS):

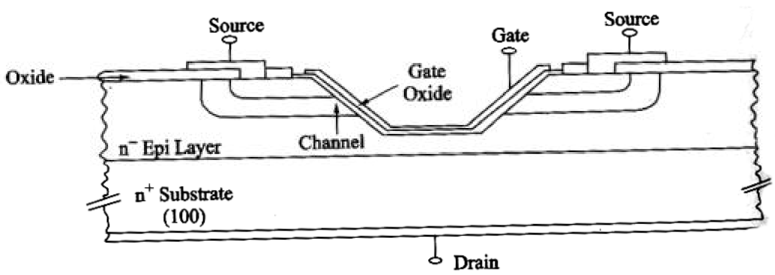


Fig 5.38 V -MOS

* V - MOSFET is similar to E - MOSFET.
* 'V' shape provides high current handling capacity and improved frequency response.
* Creates 2 vertical MOSFET
* High reverse voltage can sustain because of low doped drain region.
* Channel length is controlled by doping densities and diffusion time.

3) T-MOSFET

* Similar to V-MOS
* Gate structure is embedded in SiO_2 layer.
* Upper surface is completely occupied by source connection.
* Lower surface is occupied by drain connection.
* Construction is easier than VMOS
* Packaging density is high than VMOS

5.13 COMPARISON BETWEEN POWER BJT & POWER MOSFET

CHARACTERISTICS	POWER BJT	POWER MOSFET
Input Impedance	Lower than MOS	Very High
Breakdown Voltage	Depends on V_{CE}	Depends on V_{DS}
Switching time	Slow due to minority carrier devices	Faster; no storage time and no influence of temperature
Temperature stability	H_{fe} rises and V_e falls with increase in temperature	Extremely high stability.

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[2] Christo Ananth, Vivek.T, Selvakumar.S., Sakthi Kannan.S., Sankara Narayanan.D, "Impulse Noise Removal using Improved Particle Swarm Optimization", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 3, Issue 4, April 2014,pp 366-370
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