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Monograph On Bipolar Junctions

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NPN - PNP - Junctions - Early effect - Current Equations - Input and Output characteristics of CE, CB, CC - Hybrid - π Model - h parameter model, Ebers Moll Model - Gummel Poon model - Multi Emitter Transistor.

2.1 INTRODUCTION:

* **BJT (BIPOLAR JUNCTION TRANSISTOR):**

Current through transistor is due to both majority and minority carriers.

* **FET (FIELD EFFECT TRANSISTOR):**

Current through transistor is due to majority carriers only.

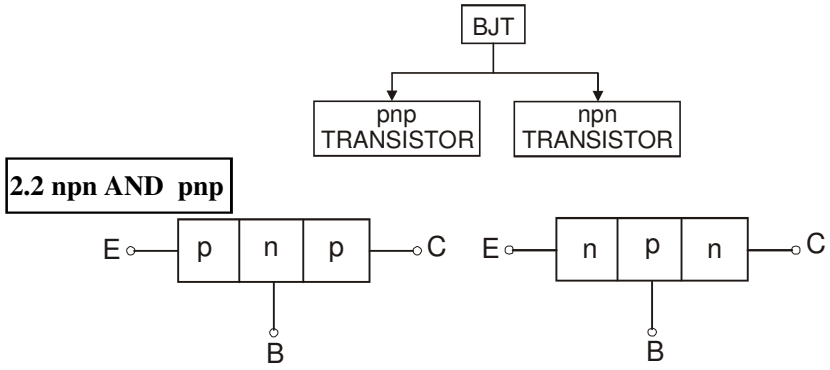

Fig 2.1 npn and pnp TRANSISTOR

* BJT is a 3 layer **semiconductor** device consisting of 2 pn junctions.

* Center layer → Base (B); left layer →Emitter (E) and right layer → Collector (C)

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* **EMITTER LAYER** is **heavily doped** and it **emits electrons** to base if transistor is of **npn type** and **emits holes** to base if transistor is of pnp type.

BASE LAYER is **lightly doped** and **COLLECTOR LAYER** is **intermediate**. (Collects electrons if transistor is of npn type or collects holes if transistor is of pnp type from base.). Christo Ananth et al.[1] discussed about principles of Semiconductors which forms the basis of Electronic Devices and Components.

TRANSISTOR WITHOUT BIAS:

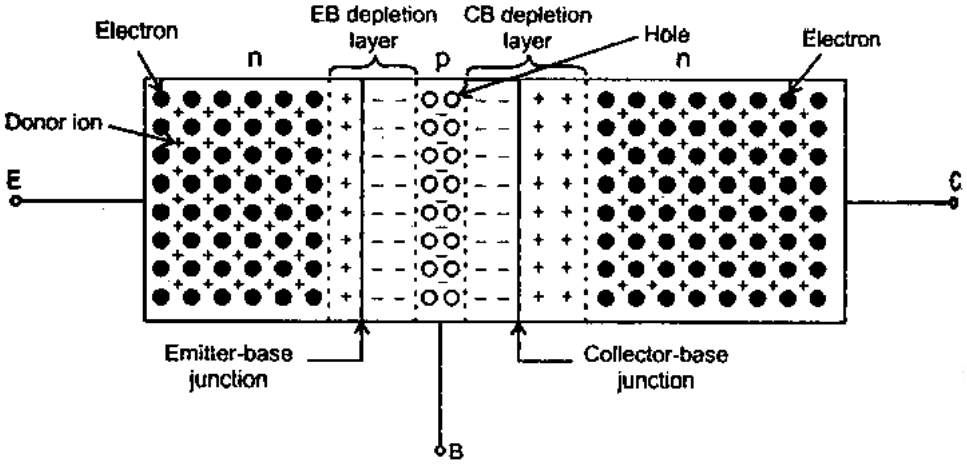

Fig 2.2TRANSISTOR WITHOUT BIAS

* In npn transistor, there are 2 junctions (Emitter base junction and Collector base junction)

* By Repulsion, free electrons on n side diffuse across Emitter base junction and recombine with holes in base.

* Electrons in collector diffuse across Collector base junction.

* When free electron in n-layer diffuse across junction, pentavalent atoms are formed in n layer and make it positive ion.

* After diffusion, it combines with parent trivalent atom in p-region making it negative. So, layer of depleted carriers is formed at the junction.

This layer of depletion without free charge carriers is called **"depletion layer".**

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* Beyond a certain point, depletion layer acts like a barrier to diffusion of free electron across junction. Difference of potential across diffusion layer is called "**BARRIER POTENTIAL**"

* EMITTER → HEAVILY DOPED ⇒ Depletion layer penetrates lightly into emitter region.
* BASE → LIGHTLY DOPED ⇒ Depletion layer penetrates deeply into base.
* COLLECTOR → MODERATELY DOPED ⇒ Depletion layer penetrates moderately into collector
* Depletion layer width in Collector base junction > Depletion layer width in Emitter base junction.

TRANSISTOR WITH BIAS (May /June - 2014 - 2 Marks)

a) TRANSISTOR WITH EMITTER BASE & COLLECTOR BASE JUNCTIONS FORWARD BIASED:

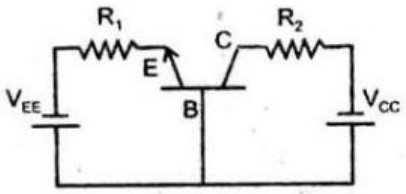
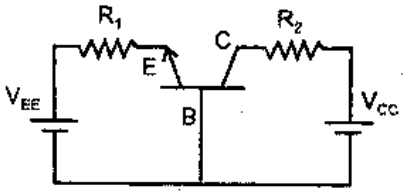


Fig.2.3 TRANSISTOR WITH EB & CB JUNCTIONS FORWARD BIASED

b) TRANSISTOR WITH EMITTER BASE & COLLECTOR BASE JUNCTION REVERSE BIASED:



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c) TRANSISTOR WITH EMITTER BASE JUNCTION FORWARD BIASED AND COLLECTOR BASE JUNCTION REVERSE BIASED

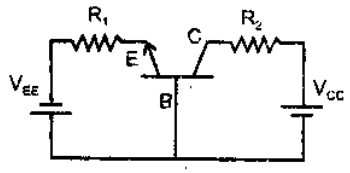


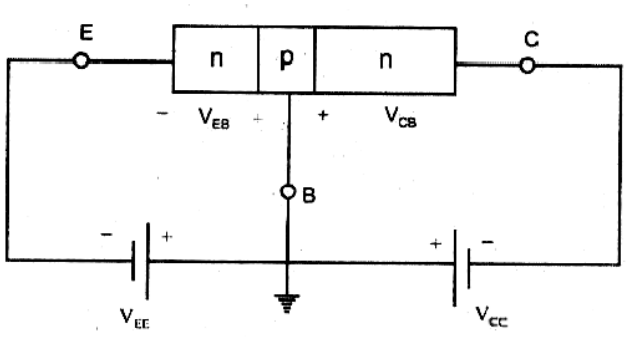
Fig. 2.5 TRANSISTOR WITH EB JUNCTION FORWARD BIASED AND CB JUNCTION REVERSE BIASED

→ 2 *pn* junctions must be correctly biased with external dc voltages.
→ In Fig. 2.3, Both EB and CB junctions are forward biased ⇒Emitter and Collector currents are large.
→ In Fig. 2.4, Both EB and CB junctions are reversed biased⇒ Emitter and Collector currents are due to thermally generated minority carriers.
→ In Fig. 2.5, Emitter base junction is forward biased and Collector base junction is reverse biased.

x

2.2.3 OPERATION OF npn TRANSISTOR

a) TRANSISTOR WITH FORWARD BIASED EB JUNCTION AND CB JUNCTION.



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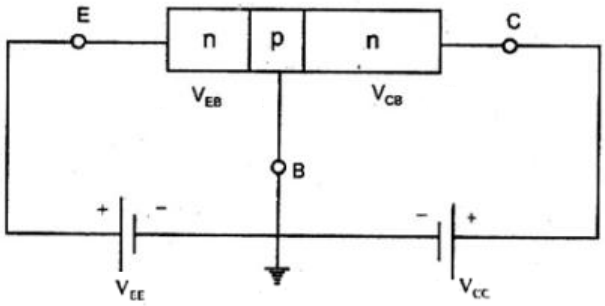
b) TRANSISTOR WITH EB JUNCTION AND CB JUNCTION REVERSE BIASED



c) TRANSISTOR WITH EB JUNCTION FORWARD BIASED AND CB JUNCTION REVERSE BIASED

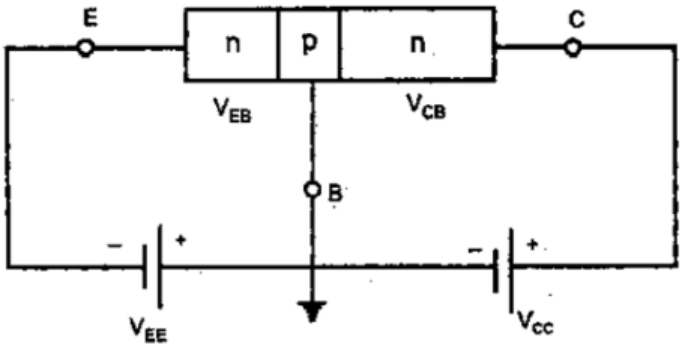


Fig 2.8 TRANSISTOR WITH EB JUNCTION FORWARD BIASED AND CB JUNCTION REVERSE BIASED

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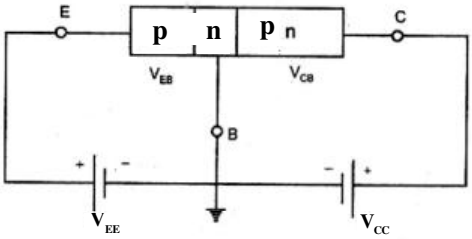
* In Fig 2.6, EB & CB junctions are forward biased ⇒Barrier potential at EB junction and CB junction reduces ⇒Electrons flow from n-type to p- type.
* In Fig 2.7, EB & CB junctions are reverse biased⇒ Emitter and collector currents are due to thermally generated minority carriers.
* In Fig 2.8, when EB junction is forward biased, Barrier potential reduces ⇒Electrons flow from n- type emitter to p-type base. Since Base is thin and lightly doped, small portion of base electrons recombines with holes and constitutes base current.

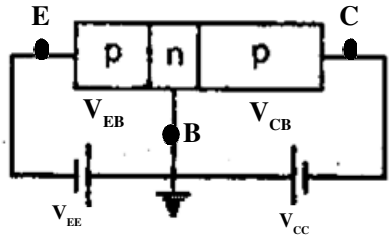
X

2.2.4 OPERATION OF PNP TRANSISTOR

a) pnp TRANSISTOR WITH EB JUNCTION & CB JUNCTION FORWARD BIASED:



b) pnp TRANSISTOR WITH EB JUNCTION & CB JUNCTION REVERSE BIASED:



C) pnp TRANSISTOR WITH EB JUNCTION FORWARD BIASED & CB

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JUNCTION REVERSE BIASED

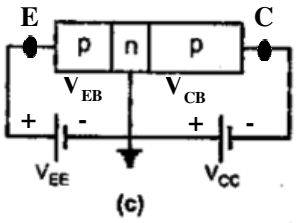


Fig. 2.11 pnp TRANSISTOR WITH EB JUNCTION FORWARD BIASED & CB JUNCTION REVERSE BIASED

* In Fig 2.9, Both EB and CB junctions are forward biased⇒ Emitter and and Collector currents are large.

* In Fig 2.10, Emitter Base junction and Collector Base junction are reverse biased ⇒ Emitter and Collector currents are small due to thermally generated minority carriers.

* In Fig 2.11, Emitter base junction is forward biased ⇒Lot of holes cross from emitter region to collector region.

  Since base is thin and lightly doped, small portion of base electrons recombines with holes and constitutes small base current.

X

2.3 CURRENT EQUATIONS

CURRENTS IN TRANSISTOR:

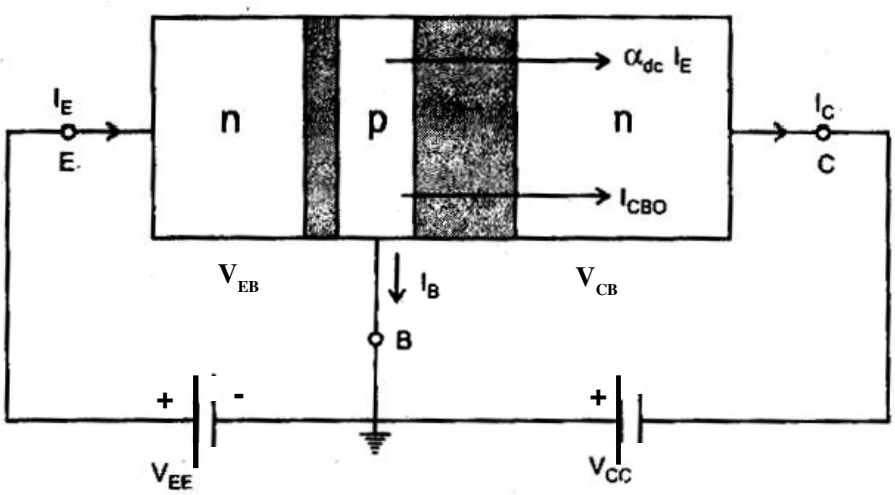
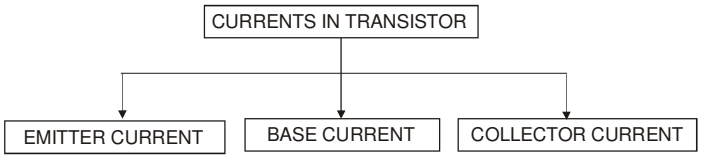


Fig 2.12 CURRENTS IN TRANSISTOR

* EB junction is forward biased and CB junction is reverse biased.



COLLECTOR CURRENT:

$$I_c = \square_{dc} I_E + I_{CBO} \rightarrow ①$$

→ Current which leaves Collector base junction = $\square_{dc} I_E$

→ Collector base junction is reverse biased

$\Rightarrow$ Minority carriers in base move across junction and constitutes small reverse saturation current called as "**COLLECTOR TO BASE LEAKAGE CURRENT** (I_{CBO})"

From ①, $\square_{dc} = \frac{I_c}{I_E}$

$\because I_{CBO} << I_C$,

COMMON BASE CURRENT GAIN, $\boxed{\square_{dc} \approx \frac{I_C}{I_E}}$ $\rightarrow$②

$\rightarrow$ Common base current gain ($\square_{dc}$) is defined as the ratio of Collector current to Emitter current.

$\rightarrow$ Collector current I_c is controlled by base emitter voltage.

$\therefore \boxed{I_c = I_{sc} \exp \frac{V_{BE}}{V_T}}$ ($I_{sc} \rightarrow$ Source current in collector side)

EMITTER CURRENT

$\rightarrow$ Current due to flow of holes from Emitter to base when EB junction is forward biased.

$\boxed{I_E = I_C + I_B}$

Emitter current $\boxed{I_E = I_{SE} \exp \frac{V_{BE}}{V_T}}$

I_{SE} →Source current in emitter side

BASE CURRENT:

$$\boxed{I_C = \square_{dc} I_B + I_{CEO}} \qquad \rightarrow ③$$

$$\square_{dc} = \frac{I_C}{I_B}$$

$I_{CEO} << I_C$,

$$\boxed{\square_{dc} \approx \frac{I_C}{I_B}} \qquad \rightarrow ④$$

→ Common Emitter current gain ($\square_{dc}$)is defined as the ratio of Collector current to Base current.

→ Base current I_B is controlled by base emitter voltage.

$\boxed{I_B = I_{SB} \exp \frac{V_{BE}}{V_T}}$; I_{SB}→ Source current in base.

x

2.3.4 CURRENT EQUATIONS:

* Current Equations of BJT can be derived from current equations in a junction diode.

* Consider forward biased pn junction. By applied voltage, holes are injected into n-side and electrons into p-side of diode.

Let $p_n'(x)$ → increase in minority carrier concentration above equilibrium

p_{n0} → hole concentration in n-side at equilibrium.

p_n → decrease in hole concentration due to recombination.

$$\boxed{p_n'(x) = p_n - p_{n0}}$$

Continuity equation states that

Rate of change of hole concentration = Sum of all increase in hole concentration

$$\frac{dp}{dt} = \frac{p_{n0} - p_n}{\square_p} - \frac{1}{q}\frac{dJ_p}{dx}$$

For steady state,

$$\frac{dp}{dt} = 0$$

$$\therefore 0 =$$

$$p_{n0} - p_n \qquad -\frac{1}{\tau_p}\frac{dJ_p}{q\ dx}$$

$$\frac{1}{q}\frac{dJ_p}{dx} = \frac{p_{n0} - p_n}{\tau_p}$$

$$\frac{dJp}{dx} = \frac{q(p_{n0} - p_n)}{\tau_p} \rightarrow ①$$

Hole diffusion current density

$$J_p \propto \frac{dp}{dx}$$

$$J_p = -q\ D_p \frac{dp}{dx} \quad (D_p \rightarrow \text{diffusion constant for holes})$$

Hole diffusion current density $J_p = -q D_p \frac{dp_n}{dx}$ $\rightarrow$②

Subs② in ①

$$\frac{d}{dx}\left(-qD_p \frac{dp_n}{dx}\right) = q\left(\frac{p_{n0} - p_n}{\tau_p}\right)$$

$$-qD_p \frac{d^2 p_n}{dx^2} = \frac{q(p_{n0} - p_n)}{\tau_p}$$

$$\frac{d^2 p_n}{dx^2} = \frac{-(p_{n0} - p_n)}{D_p \tau_p}$$

$$\frac{d^2 p_n}{dx^2} = \frac{p_n - p_{n0}}{D_p \tau_p}$$

Diffusion length for holes (L_p), (Average distance travelled by hole before recombination)

$$L_P = (D_p \tau_p)^{1/2}$$

$$\frac{d^2 p_n}{dx^2} = \frac{p_n - p_{n0}}{L_p^2}$$

Since $p_n' = p_n - p_{n0}$

$$\frac{d^2 p_n}{dx^2} = \frac{p_n'(x)}{L_p^2}$$

Solution of this equation is given by $p_n'(x) = k_1 e^{-x/L_p} + k_2 e^{x/L_p}$ (where $k_1, k_2 \rightarrow$constants)

To find k_1 and k_2:

At $x = \infty$, $p_n'(x) = 0$

$\therefore 0 = 0 + k_2$

$\boxed{k_2 = 0}$

At $x = 0$,

$p_n'(0) = k_1 \Rightarrow \boxed{k_1 = p_n'(0)}$

$\therefore p_n'(x) = p_n'(0) e^{-x/L_p} + 0$

$= p_n'(0) e^{-x/L_p}$

$= (p_n(x) - p_{n0}) e^{-x/L_p}$ $\rightarrow$③

Diffusion current,

$$I_{pn}(x) = AJ_p$$

$$= A(-qD_p \frac{dp_n}{dx})$$

$$= -qAD_p \frac{d}{dx}(p_n) \qquad \rightarrow ④$$

We have $p_n'(x) = p_n - p_{n0}$

$$p_n = p_n'(x) + p_{n0}$$

$$\frac{dp_n}{dx} = \frac{dp_n'(x)}{dx}$$

$$\therefore ④ \Rightarrow I_{pn}(x) = -qAD_p \frac{dp_n'(x)}{dx}$$

$$= -qAD_p \frac{d}{dx}\left[(p_n(x) - p_{n0})e^{-x/L_P}\right] \qquad (\because \textit{from } ③)$$

$$= \frac{-qAD_p p_n'(0)e^{-x/L_P}}{L_P}$$

$$I_{pn}(x) = \frac{qAD_p}{L_p} p_n'(0) e^{-x/L_P}$$

$$I_{pn}(x) = \frac{AqD_p}{L_p}(p_n(0) - p_{n0})e^{-x/L_P}$$

Minority diffusion current crossing junction at $x = 0$ is

$$I_{pn}(0) = \frac{AqD_p}{L_p}(p_n(0) - p_{n0})$$

$$\boxed{I_{pn}(0) = \frac{AqD_p}{L_p} p_n'(0)}$$

And total current density for hole is J_p=Drift current + Diffusion current density for holes

$$J_p = \left[qp\mu_p E \right] - \left[qD_p \frac{dp}{dx} \right]$$

↓ ↓

Drift current density for holes + Diffusion current Density for holes

$$\boxed{J_p = qp\mu_p E - qD_p \frac{dp}{dx}}$$

Einstein's relation states that

At fixed temperature, Ratio of diffusion constant to mobility is constant

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = kT$$

where T → Temperature in ºK

k → Boltzmann constant in eV/ºK

Voltage equivalent temperature $\boxed{V_T = KT}$

Junction potential $\boxed{V_j = V_0 - V}$

Electric field intensity, $E = \frac{V_T}{p}\frac{dp}{dx} = \frac{-dV}{dx}$

$$\Rightarrow \frac{dp}{p} = \frac{-dV}{V_T}$$

$$\int_{P_{p0}}^{p_n(0)} \frac{dp}{p} = -\int_0^{V_j} \frac{dV}{V_T}$$

$$\ln\left(\frac{p_n(0)}{p_{p0}}\right) = \frac{-1}{V_T}(V_j)$$

$$\ln\left(\frac{p_n(0)}{p_{po}}\right) = \frac{-1}{V_T}(V_0 - V)$$

$$\boxed{p_n(0) = p_{p0} e^{-(V_0 - V)/V_T}} \quad \rightarrow ⑤$$

By **Law of Junction,**

$$V_0 = V_T \ln \frac{p_{p0}}{p_{n0}}$$

$$\frac{V_0}{V_T} = \ln \frac{p_{p0}}{p_{n0}}$$

$$e^{V_0/V_T} = \frac{p_{p0}}{p_{n0}}$$

$$\boxed{p_{p0} = p_{n0}\, e^{V_0/V_T}} \quad \rightarrow ⑥$$

Subs ⑥in⑤,

$$p_n(0) = p_{n0} e^{V_0/V_T}\ e^{-(V_0 - V)/V_T}$$

$$= p_{n0}\, e^{(V_0 - V_0 + V)/V_T}$$

$$\boxed{p_n(0) = p_{n0}\, e^{V/V_T}}$$

We know that

$$I_{pn}(0) = \frac{AqD_p}{L_p} p_n'(0)$$

$$= \frac{AqD_p}{L_p}(p_n(0) - p_{n0})$$

$$= \frac{AqD_p}{L_p}(p_{n0}\, e^{V/V_T} - p_{n0})$$

$$\boxed{I_{pn}(0) = \frac{AqD_p\, p_{n0}}{L_p}(e^{V/V_T} - 1)}$$

$$\boxed{I_{np}(0) = \frac{AqD_n n_{p0}}{L_n}(e^{V/V_T} - 1)}$$

$$I = I_{pn}(0) + I_{np}(0)$$

$$= \frac{AqD_p\, p_{n0}}{L_p}(e^{V/V_T} - 1) + \frac{AqD_n\, n_{p0}}{L_n}(e^{V/V_T} - 1)$$

$$I = I_0(e^{V/V_T} - 1)$$

where $I_0 = \frac{AqD_p\, p_{n0}}{L_p} + \frac{AqD_n\, n_{p0}}{L_n}$

REVERSE SATURATION CURRENT:

$$I_0 = Aq\left(\frac{D_p p_{n0}}{L_p} + \frac{D_n n_{p0}}{L_n}\right)$$

$$p_{n0} = \frac{n_i^2}{N_D} \text{ and } n_{p0} = \frac{n_i^2}{N_A}$$

$$I_0 = Aq\left(\frac{D_p n_i^2}{L_p N_D} + \frac{D_n n_i^2}{L_n N_A}\right)$$

$$\boxed{I_0 = Aq\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) n_i^2}$$

Diode current Equation:

Applied Voltage and current are related by $I = I_0 (e^{V/\square V_T} - 1)$

where I_0 = reverse saturation current
V = applied voltage
I = diode current
V_T = Volt equivalent temperature

$$= \frac{KT}{q}$$

At any temperature

$$V_T = \frac{1.38\times10^{-23}\times T}{1.602\times10^{-19}} = \frac{T}{11,600}$$

At room temperature,

$$V_T = \frac{300}{11,600} = 26mV$$

$\eta = 1$ for Germanium

$\eta = 2$ for Silicon

For forward bias voltage,

Current Equation is

$$I = I_0 (e^{V/\square V_T})$$

For reverse bias voltage

Current Equation is

$$\boxed{I = I_0 (e^{-V/\eta V_T} - 1)}$$

Note :

$$I = I_0(e^{V/V_T} - 1)$$

$$I = Aq\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) n_i^2 (e^{V/V_T} - 1)$$

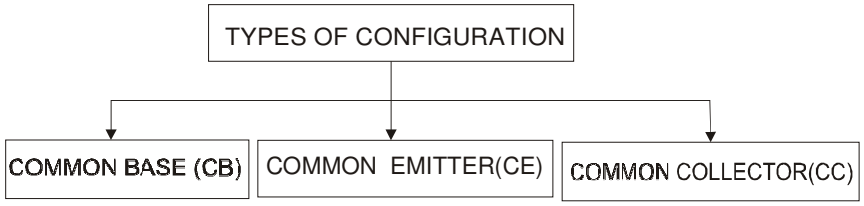
$$J = \frac{I}{A} = qn_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)(e^{V/V_T} - 1)$$

$$= qn_i^2\left(\frac{D_p}{\sqrt{D_p \tau_p} N_D} + \frac{D_n}{\sqrt{D_n \tau_n} N_A}\right)(e^{V/V_T} - 1)$$

$$J = qn_i^2\left(\sqrt{\frac{D_p}{\tau_p}}\frac{1}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{1}{N_A}\right)(e^{V/V_T} - 1)$$

x

2.4 INPUT AND OUTPUT CHARACTERISTICS OF CE, CB AND CC CONFIGURATION (May /June 2014 -16 Marks)



2.4.1 COMMON BASE CONFIGURATION:

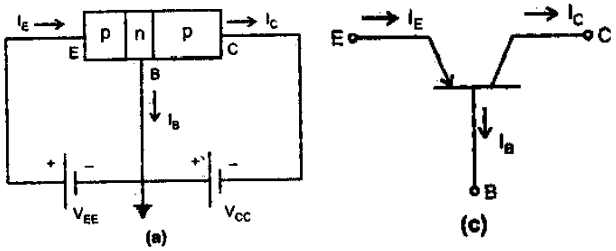


Fig 2.13 pnp TRANSISTOR

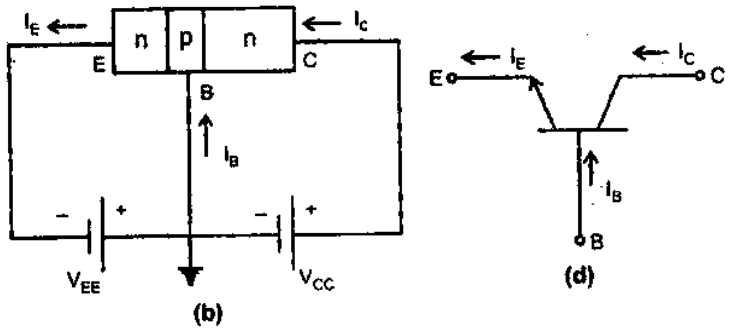


Fig 2.14 npn TRANSISTOR

→ Base is common to both input and output terminals. Base is close to ground potential.

→ **Input and Output characteristics** explains the behaviour of transistor.

A) CIRCUIT ARRANGEMENT:

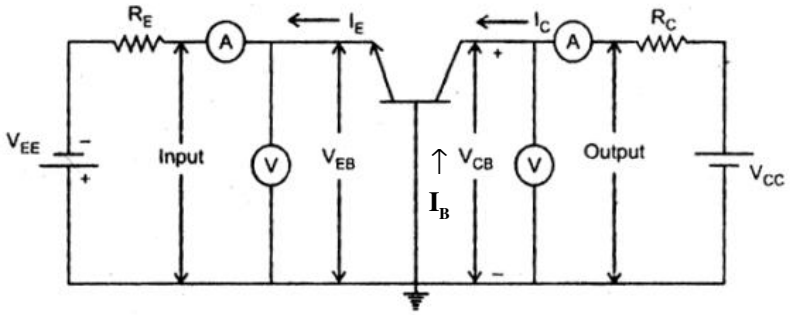


Fig 2.15 CIRCUIT ARRANGEMENT

B) INPUT CHARACTERISTICS

* Relates i/p current (I_E)to i/p voltage(V_{BE}) for different values of o/p voltage (V_{CB})

* Output voltage (V_{CB})is kept fixed and input voltage (V_{BE})is varied in steps and corresponding input current (I_E)is recorded.

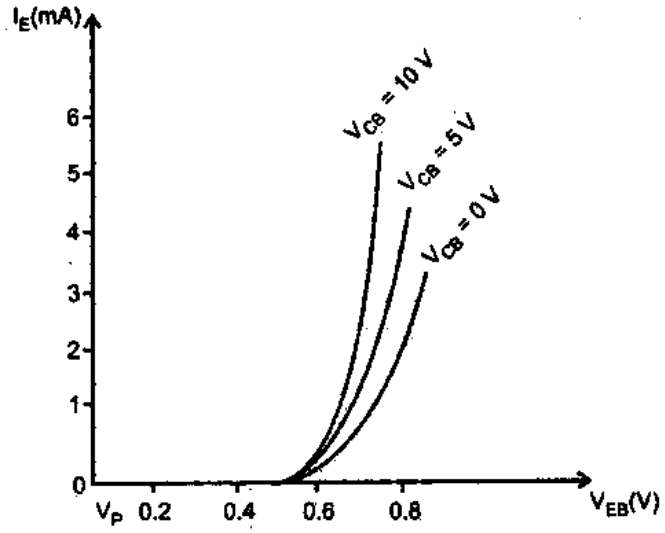
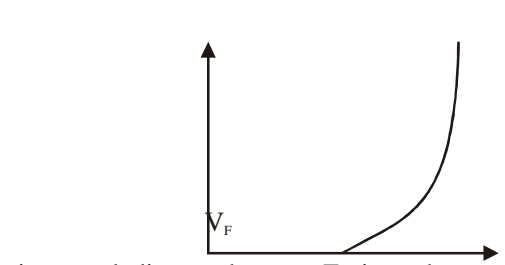


Fig 2.16 Input Characterstics

* When output voltage is 0, Emitter base junction is forward biased and so input characteristics are closed to forward biased pn junction diode.



* When V_{CB} is increased, distance between Emitter - base and Collector base depletion region reduces which reduces resistance between 2 regions. So V_{CE} increases.

C) OUTPUT CHARACTERISTICS:

→Plot between Collector to base voltage and Collector current for various levels of Emitter current.

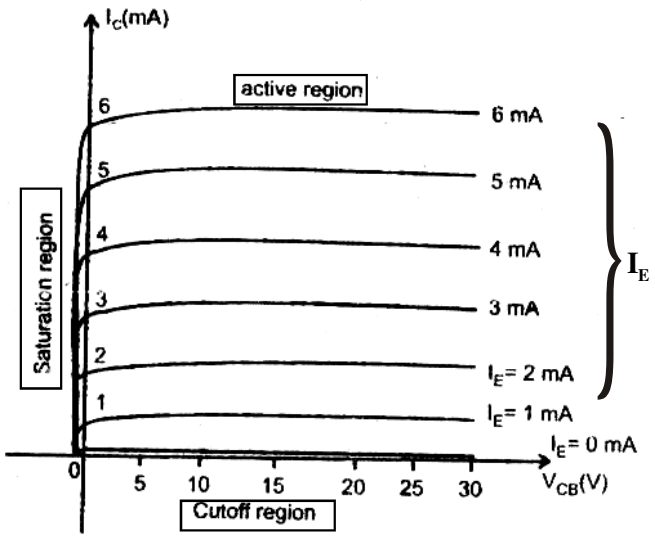


Fig 2.17 OUTPUT CHARACTERISTICS

1. ACTIVE REGION:

* Used for operating transistor as an amplifier
* Emitter-base junction is forward biased and Collector base junction is reverse biased. As I_E increases, I_C increases

$$I_C \simeq I_E \quad (if \ \alpha_{dc} \approx 1)$$

2. SATURATION REGION:

* Emitter base and Collector base junctions are forward biased.
* Region that lies to left of V_{CB} =0

* When CB junction is forward biased, flow of charge carriers is reduced $\Rightarrow$ I_C reduces to 0.

3. CUT OFF REGION

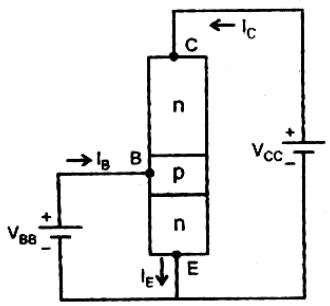
* Emitter base and collector base junctions are reverse biased.

* Region where $I_C = 0$

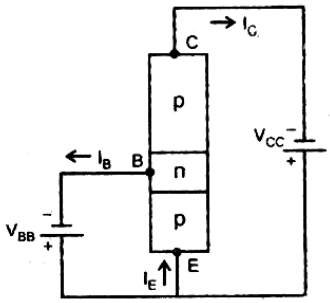
X

2.4.2. COMMON EMITTER CONFIGURATION:

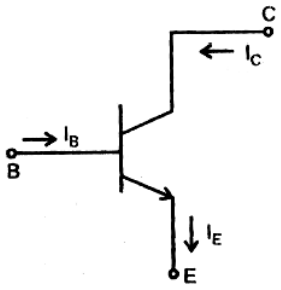
Emitter current is common to both input and output terminals.



npn TRANSISTOR



pnp TRANSISTOR



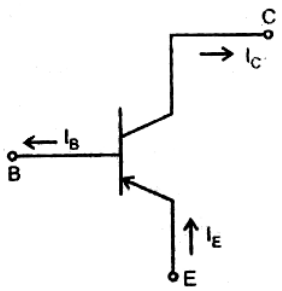


Fig . 2.18 (a) npn TRANSISTOR (b) pnp TRANSISTOR

a) CIRCUIT ARRANGEMENT:

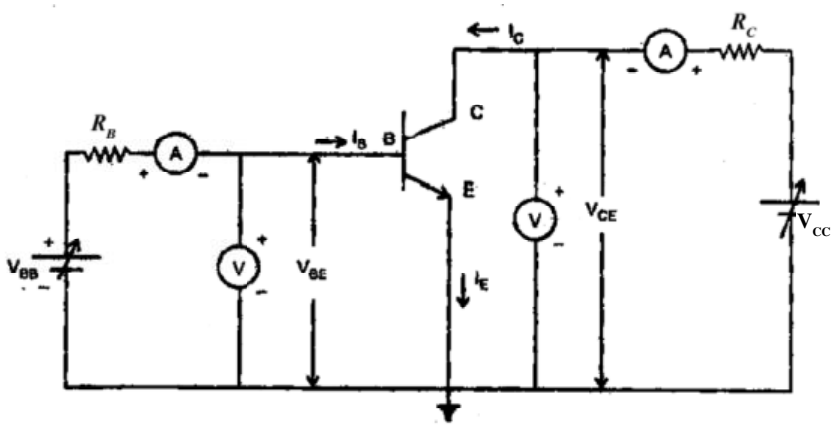


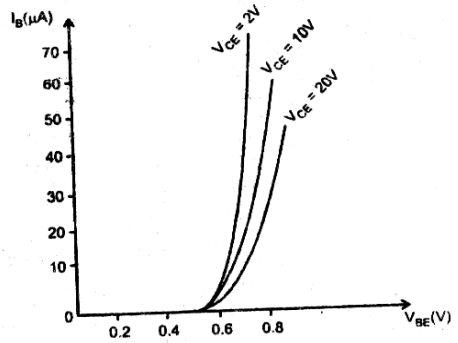
Fig 2.19 CIRCUIT ARRANGEMENT

b) INPUT CHARACTERISTICS:

* Plot between input current (I_B) and input voltage (V_{BE}) for various values of output voltage (V_{CE})
* Till cutin voltage, Base current is zero and increases exponentially as V_{BE} increases.
* When V_{CE} increases, Width of depletion region increases $\Rightarrow$ Base current decreases for constant V_{BE}.

c) OUTPUT CHARACTERISTICS:

Plot of Collector to Emitter voltage (V_{CE}) to Collector current (I_C)for constant base current(I_B)



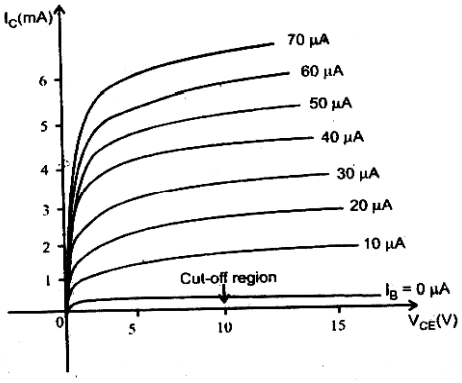


Fig 2.20 a) Input charactertics **b) Output characteristics**

1. **Active Region:**

   Base Emitter junction is forward biased and Collector base junction is reverse biased.

   When $V_{CE} = 0$, I_c is small.

2. **Saturation Region:**

   Emitter base junction and collector base junctions are forward biased.

   Increase in base current I_B produces increase in I_C.

   V_{CE} in saturation region ($V_{CE,sat} \simeq 0.2V$)

3. **Cut off Region:**

   Emitter base junction and Collector base junctions are reverse biased.

$$I_C = \alpha_{dc} I_E + I_{CB0} \rightarrow ①$$

$$I_C = \beta_{dc} I_B + I_{CE0} \rightarrow ②$$

When $I_E = 0$, $I_C = I_{CBO}$

When $I_B = 0$, $I_C = I_{CEO}$

I_{CEO} and I_{CBO} are related by

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha_{dc}}$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

x

COMMON COLLECTOR CONFIGURATION:

* Collector terminal is common to both input and output terminals.
* It has high input impedance and low output impedance.

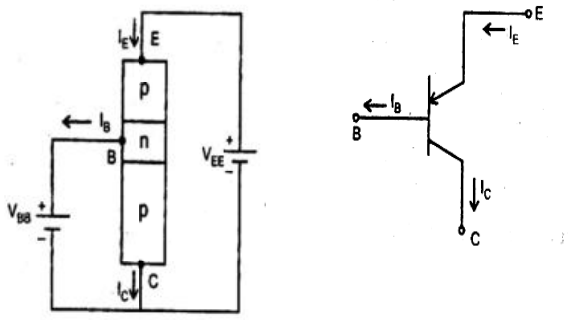
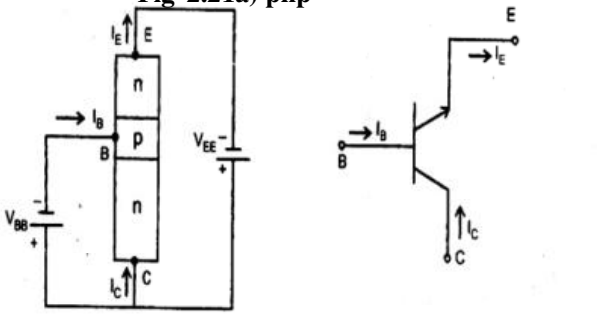


Fig 2.21a) pnp TRANSISTOR



b) npn TR ANSISTOR

A) CIRCUIT ARRANGEMENT

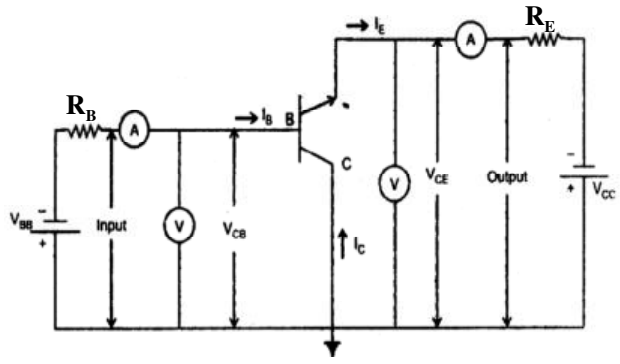


Fig 2.22 CIRCUIT ARRANGEMENT

B) INPUT CHARACTERISTICS:

→ Plot of Base current (I_B)and Collector to Base Voltage (V_{CB})

→ When V_{CB} increases, base current I_B decreases and reduces to 0.

C) OUTPUT CHARACTERISTICS:

→ Plot between I_E and V_{CE}

→ $I_C \approx I_E$ ($\therefore$ Common collector output characteristics similar to Common emitter output)

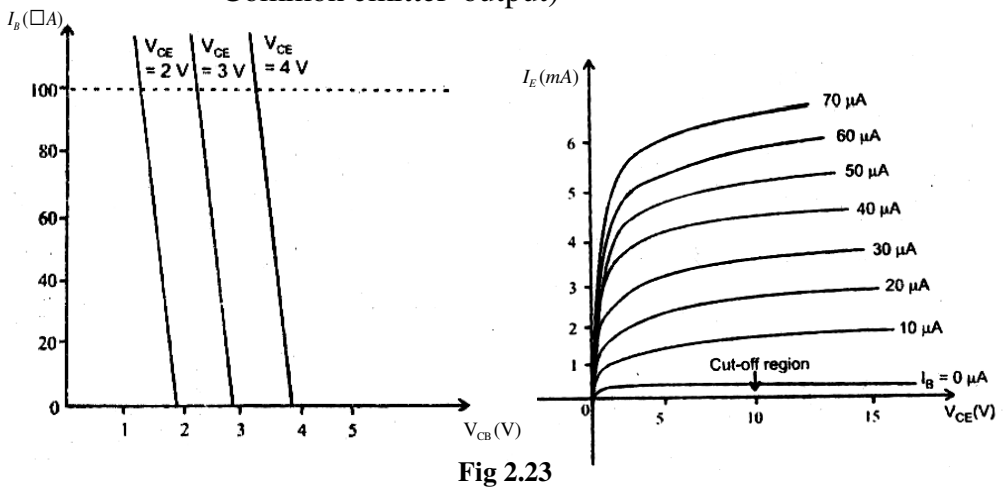


Fig 2.23

a) INPUT CHARACTERISTICS **b) OUTPUT CHARACTERISTICS**

X

DEFINITION OF □, □, □ :

A) LARGE SIGNAL CURRENT GAIN (□) [CURRENT AMPLIFICATION FACTOR]:

→ Ratio of change in Collector current (ΔI_C) to change in emitter current (ΔI_E) at constant V_{CB}

$$\alpha = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{Constant}}$$

B) TRANSPORT FACTOR (□):

→ Ratio of change in Collector current (ΔI_c) to change in base current (ΔI_B) at constant V_{CE}

$$\square = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{Constant}}$$

C) EMITTER EFFICIENCY ( ):

Ratio of change in Emitter current (ΔI_E) to change in base current (ΔI_B) at constant V_{CE}

$$= \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{CE}} = \text{Constant}$$

x

RELATIONSHIP BETWEEN(, ,)

A) REL ATION BETWEEN α AND γ:

$$I_E = I_B + I_C$$
$$I_B = I_E - I_C$$
$$\Delta I_B = \Delta I_E - \Delta I_C$$
$$\div \, by \, \Delta I_C,$$
$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C} - \frac{\Delta I_C}{\Delta I_C}$$

We know that $\boxed{= \frac{\Delta I_C}{\Delta I_E}}$ *and* $\boxed{= \frac{\Delta I_C}{\Delta I_B}}$

$$\frac{1}{} = \frac{1}{} - 1 \qquad \rightarrow ①$$

$$\boxed{= \frac{}{1-}} \qquad \rightarrow ② \qquad (\text{ in terms of })$$

From ①, $\frac{1}{} - 1 = \frac{1}{}$

$$\frac{1}{} = \frac{1}{} + 1$$

$$\square = \frac{\square}{1+\square} \qquad \rightarrow ③ \quad (\square \text{ in terms of } \square)$$

B) RELATION BETWEEN □ AND γ:

We know that $I_E = I_B + I_C$

$$I_B = I_E - I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

$\div$ by ΔI_B, $1 = \frac{\Delta I_E}{\Delta I_B} - \frac{\Delta I_C}{\Delta I_B}$

We have $\square = \frac{\Delta I_E}{\Delta I_B}$ *and* $\square = \frac{\Delta I_C}{\Delta I_B}$

$$1 = \square - \square$$

$$\square = 1 + \square \qquad \rightarrow ④ \ (\square \text{ in terms of } \square)$$

We know that $\square = \frac{\square}{1-\square}$

$$\square = 1 + \frac{\square}{1-\square} \ (\because \text{from } ④)$$

$$\square = \frac{1}{1-\square} \ (\square \text{ in terms of } \square)$$

x

COMPARISON BETWEEN CE, CC AND CB CONFIGURATIONS

COMMON BASE(CB) CONFIGURATION	COMMON EMITTER (CE) CONFIGURATION	COMMON COLLECTOR (CC) CONFIGURATION
I/P resistance-"Low"	I/p resistance - "MODERATE"	I/P resistance-"HIGH"
O/P resistance-"HIGH"	O/p resistance - MODERATE"	O/p resistance-"LOW"
CURRENT GAIN → UNITY	CURRENT GAIN → HIGH	CURRENT GAIN → HIGH
Voltage gain is low	Voltage gain is high	Voltage gain is almost unity

x

PROBLEM :1

Determine the value of base current of common base configuration whose current amplification factor is 0.92. Emitter current is 1mA.

Solution:

Given :

$I_E = 1\times10^{-3}A$

$\alpha = 0.92$

$$\alpha = \frac{I_C}{I_E}$$

$$0.92 = \frac{I_C}{1\times10^{-3}}$$

$$I_C = 0.92 \times 10^{-3}$$

$$I_E = I_B + I_C$$

$$I_B = I_E - I_C$$

$$= (1\times10^{-3}) - (0.92 \times 10^{-3})$$

$$= 0.08 \times 10^{-3}$$

$$\boxed{I_B = 0.08mA}$$

x

PROBLEM :2 At V_{CE}=7.5V, change in collector current is 1.2mA for change in base current of 20 μ A. Find β of transistor.

Solution:

Given :

At V_{CE}= 7.5V

$$\Delta I_C = 1.2\times10^{-3} A$$

$$\Delta I_B = 20\times10^{-6} A$$

$$\beta = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}}$$

$$= \frac{1.2 \times10^{-3}}{20 \times10^{-6}}$$

$$\boxed{\beta = 60}$$

x

2.5 EARLY EFFECT OR BASE WIDTH MODULATION

→ If actual Base width is W_B and width of depletion region is W,

Effective electrical base width $W_B' = W_B - W$

→ Dependency of Base width on Collector Reverse bias is known as **"EARLY EFFECT"**

→ Base width varies with increase in reverse Collector voltage, so early effect is also known as **"BASE WIDTH MODULATION"**

→ Early effect can be seen in current voltage characteristics.

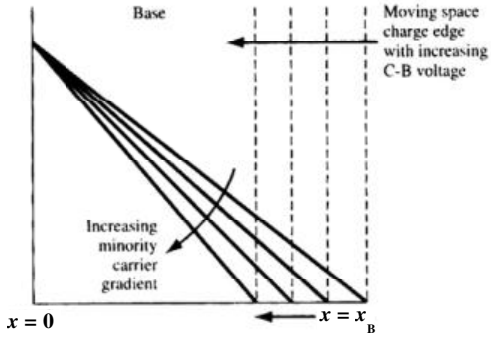
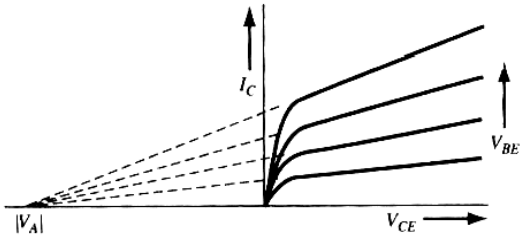


Fig 2.24 Change in base width and Change in Minority carrier Gradient with Change in B-C space Charge width

→ Reduction in base width ⇒ Increase in Gradient in minority carrier concentration

⇒ Increase in diffusion current.



(Early Voltage)

Fig 2.25 I_C Vs V_{CE} showing Early Effect and Early Voltage

→ Early effect produces non zero slope ⇒ finite output conductance (g_0)

→ If Collector current is 0, curves interest voltage axis at a point called as "**EARLY VOLTAGE**"

$$\therefore \frac{dI_C}{dV_{CE}} = \frac{I_C}{V_{CE} \square_A} = g_0$$

$$\Rightarrow \boxed{I_C = g_0 (V_{CE} + V_A)}$$

2.5.1 EFFECTS OF BASE WIDTH MODULATION:

* As Base Width decreases ⇒ No.of Majority carriers that recombine with minority carriers decreases ⇒ Base current decreases.

* As Base width decreases, concentration gradient of minority carriers increases.

* For large reverse bias, Base width may be reduced to zero ⇒ Voltage breakdown in transistor. This is called **"PUNCH THROUGH"**

2.6 BREAKDOWN IN TRANSISTORS:

1) AVALANCHE MULTIPLICATION:

* Base - Collector junction is reverse biased ⇒ Breakdown occurs called as Avalanche Breakdown.

* Avalanche Breakdown is caused by impact ionization.

* Because of High Kinetic energy, electron hole pair is generated in collector.

* By Electric field, holes are forced to base which induces electron current □ MI_C

* When □ M>1 ⇒ avalanche (unlimited increase in collector current without external control

2) REACH THROUGH (PUNCH THROUGH) :

* Increase in reverse bias ⇒ Increase in depletion region.

* Since base is lightly doped, depletion region penetrates deeper into base and undepleted part of base becomes narrower.

* Further increase in reverse bias ⇒ Depletion region spreads completely to reach emitter junction. This is known as **"REACH THROUGH"** or **"PUNCH THROUGH"**

* Decrease in Emitter base Voltage $\Rightarrow$ Emitter current increases $\Rightarrow$ **"Transistor Breakdown".**

x

2.7. HYBRID MODEL OR h- PARAMER MODEL (May /June 2010 -16 Marks)

TWO PORT NETWORK:

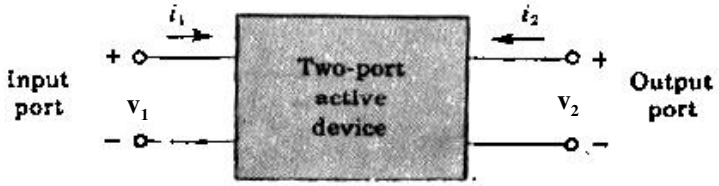


Fig 2.26 TWO PORT NETWORK

$\rightarrow$If two - port device is an ideal transformer, and if it is linear

$$\square_1 = h_{11} i_1 + h_{12} V_2 \rightarrow ①$$

$$i_2 = h_{21} i_1 + h_{22} V_2 \rightarrow ②$$

$h_{11}, h_{12}, h_{21}, h_{22} \rightarrow$h parameters or hybrid parameters.

$$h_{11} = \left.\frac{v_1}{i_1}\right|_{V_2=0} \qquad h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2=0}$$

$$h_{12} = \left.\frac{v_1}{v_2}\right|_{i_1=0} \qquad h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1=0}$$

h_{11}= input resistance h_{21}= short circuit current gain

h_{12} =Reverse open circuit voltage amplification h_{22} = Output conductance

$\rightarrow v_1, v_2, i_1, i_2$ are functions of time.

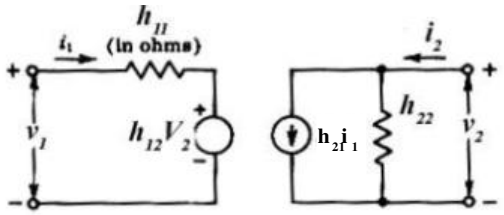


Fig 2.27 HYBRID MODEL FOR TWO -PORT NETWORK

Apply KVL to first loop,

$V_1 = h_{11}\, i_1 + h_{12}\, V_2 \quad \rightarrow ③$

Apply KCL to second loop,

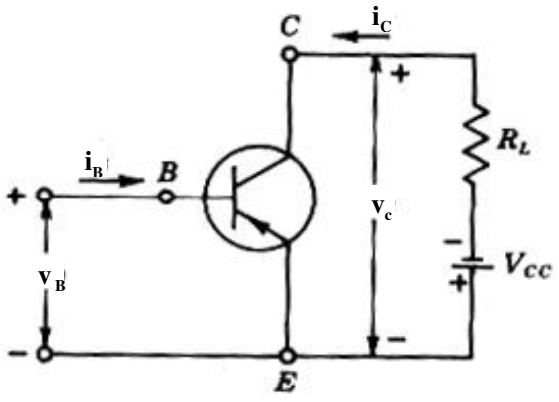
$i_2 = h_{21} i_1 + h_{22} V_2 \quad \rightarrow ④$

①=③ and ②=④

∴Hybrid model is verified. Christo Ananth et al. [2] discussed about Improved Particle Swarm Optimization. The fuzzy filter based on particle swarm optimization is used to remove the high density image impulse noise, which occur during the transmission, data acquisition and processing. The proposed system has a fuzzy filter which has the parallel fuzzy inference mechanism, fuzzy mean process, and a fuzzy composition process. In particular, by using no-reference Q metric, the particle swarm optimization learning is sufficient to optimize the parameter necessitated by the particle swarm optimization based fuzzy filter, therefore the proposed fuzzy filter can cope with particle situation where the assumption of existence of "ground-truth" reference does not hold. The merging of the particle swarm optimization with the fuzzy filter helps to build an auto tuning mechanism for the fuzzy filter without any prior knowledge regarding the noise and the true image. Thus the reference measures are not need for removing the noise and in restoring the image. The final output image (Restored image) confirm that the fuzzy filter based on particle swarm optimization attain the excellent quality of restored images in term of peak signal-to-noise ratio, mean absolute error and mean square error even when the noise rate is above 0.5 and without having any reference measures.

TRANSISTOR HYBRID MODEL:

* h parameters can be obtained from transistor static characteristic curves



i_B, i_C $\rightarrow$ instantaneous currents

V_B,V_C $\rightarrow$ instantaneous voltages

$$V_B = f_1(i_B, V_C) \quad \rightarrow ⑤$$

[V_B is a function of i_B and V_C]

$$i_c = f_2(i_B, V_C) \quad \rightarrow ⑥$$

[i_C is another function of i_B and V_C]

Taking Taylor's series expansion of ⑤and⑥

$$\Delta V_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial f_1}{\partial V_C}\right|_{I_B} \Delta V_C \rightarrow ⑦$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial f_1}{\partial V_C}\right|_{I_B} \Delta V_C \rightarrow ⑧$$

ΔV_B, $\Delta V_C \rightarrow$ small signal base and Collector voltages.

Δi_B, $\Delta i_C \rightarrow$ small signal base and Collector currents.

⑦and⑧ can be rewritten as:

$V_b = h_{ie} i_b + h_{re} V_C \quad \rightarrow ⑨$

$i_C = h_{fe} i_b + h_{oe} V_C \quad \rightarrow ⑩$

where

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{V_C}$$

$$h_{re} = \left.\frac{\partial f_1}{\partial V_C}\right|_{I_B}$$

$$h_{fe} = \left.\frac{\partial f_2}{\partial i_B}\right|_{V_C}$$

$$h_{oe} = \left.\frac{\partial f_2}{\partial V_C}\right|_{I_B}$$

} h- parameters of Common Emitter connection

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{V_C} = \left.\frac{\partial V_B}{\partial i_B}\right|_{V_C}$$

$$h_{re} = \left.\frac{\partial f_1}{\partial V_C}\right|_{I_B} = \left.\frac{\partial V_B}{\partial V_C}\right|_{I_B}$$

$$h_{fe} = \left.\frac{\partial f_2}{\partial I_B}\right|_{V_C} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C}$$

$$h_{oe} = \left.\frac{\partial f_2}{\partial V_C}\right|_{I_B} = \left.\frac{\partial i_C}{\partial V_C}\right|_{I_B}$$

h- PARAMETER MODEL FOR CE, CB, CC CONFIGURATION

$i_B+i_C+i_E = 0$

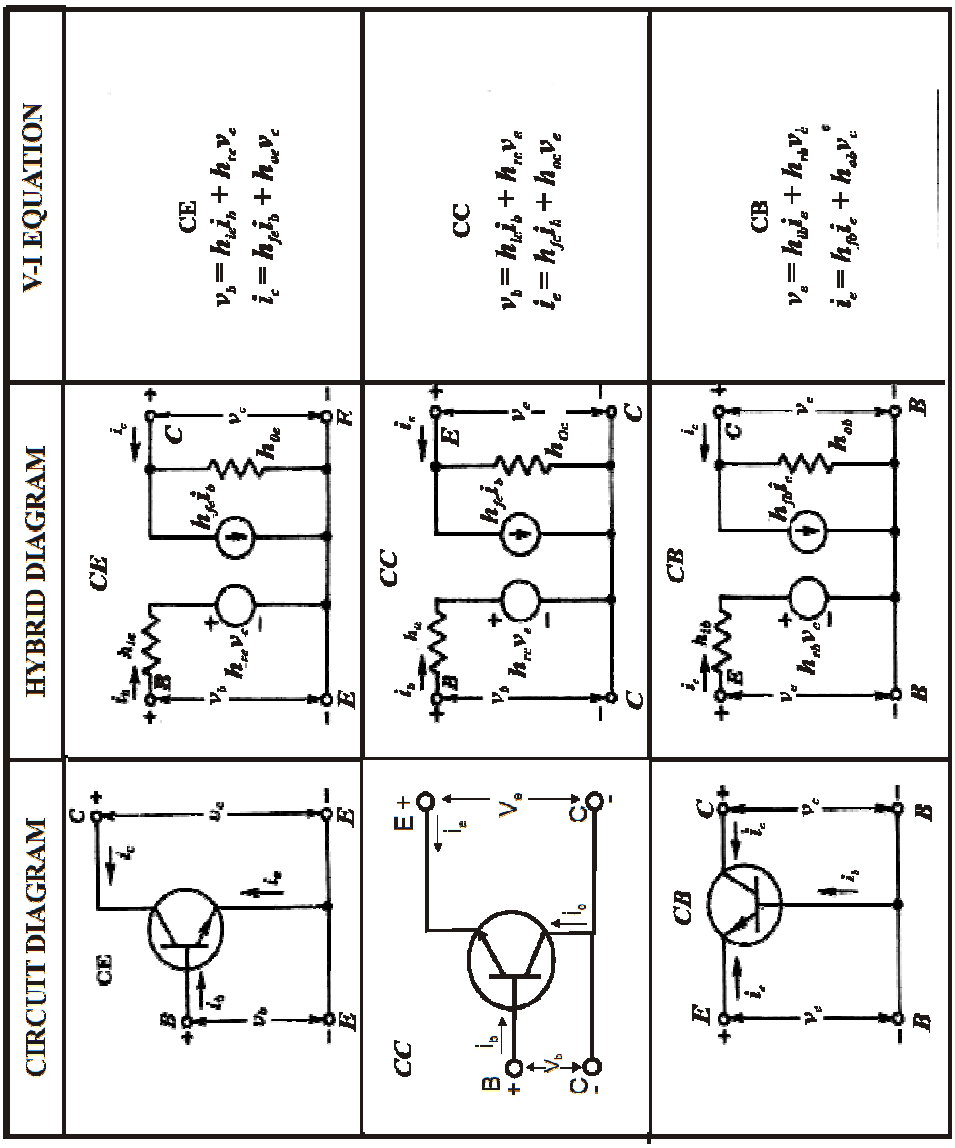


Fig 2.29 h- PARAMETER MODEL FOR CE, CB, CC CONFIGURATION (May /June 2014-2 Marks)

DETERMINATION OF h PARAMETERS FROM CHARACTERISTICS:

* **h_{fe} DETERMINATION:**

We know that $h_{fe} = \frac{\partial i_C}{\partial i_B} \approx \left.\frac{\Delta i_C}{\Delta i_B}\right|_{V_C}$

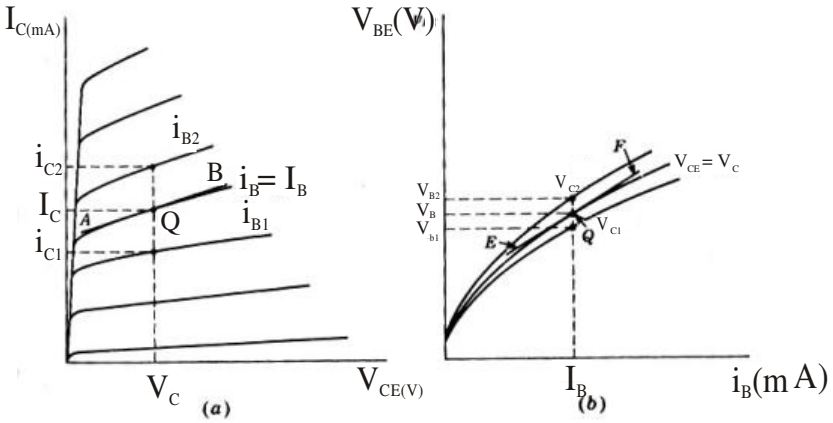


Fig 2.30 (a) CE = OUTPUT CHARACTERISTICS

(b) CE = INPUT CHARACTERISTICS

* Base currents are taken around quiescent point Q ($i_B=I_B$) and to collector voltage $V_{CE}=V_C$ around quiescent point Q.

* $$h_{fe} = \frac{i_{C2} - i_{C1}}{i_{B2} \square \quad i_{B1}}$$

A) h_{oe} DETERMINATION:

$$h_{oe} = \frac{\partial i_C}{\partial V_C} \approx \left.\frac{\Delta i_C}{\Delta V_C}\right|_{I_B}$$

* h_{oe} at quiescent point Q is given by slope of output characteristic curve at that point.

* Slope can be evaluated by drawing line AB tangential to characteristic curve at point Q. Christo Ananth et al.[3] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.

B) **h_{ie} DETERMINATION:**

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \frac{\Delta V_B}{\Delta i_B}\bigg|_{V_C}$$

* h_{ie} at quiescent point Q is given by slope of input characteristic curve at that point.

* Slope can be evaluated by drawing line EF tangential to characteristic curve at point Q

C) **h_{re} DETERMINATION:**

$$h_{re} = \frac{\partial V_B}{\partial V_C} \approx \frac{\Delta V_B}{\Delta V_C}\bigg|_{I_B}$$

* Vertical line on input characteristics represents constant base current.

$$h_{re} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

x

2.8 EBERS -MOLL MODEL

* Based on interacting diode junctions.

* Applicable to any transistor operating modes.

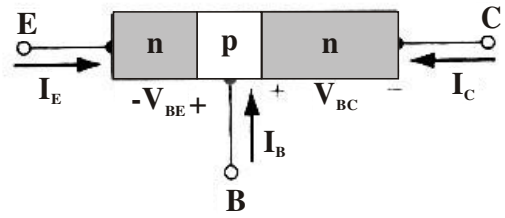


Fig 2.31 EBERS - MOLL - MODEL

$I_E+I_B+I_C=0$ $\rightarrow$①

Collector current

$$I_C=\alpha_F I_F - I_R \qquad \rightarrow ②$$

where $\alpha_F \rightarrow$common base current gain in forward active mode

Here $I_C= \alpha_F I_F + I_{CS}$ $\rightarrow ③$

where $I_{CS} \rightarrow$reverse bias B-C junction current.

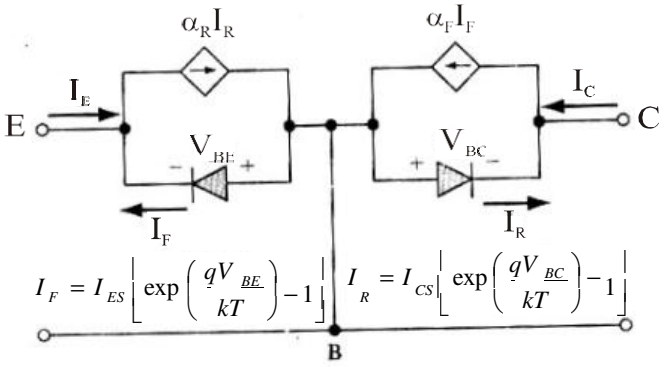


Fig 2.32 EBERS - MOLL EQUIVALENT CIRCUIT

FORWARD CURRENT, $I_F = I_{ES}\left[\exp\left(\frac{qV_{BE}}{KT}\right)-1\right]$ $\rightarrow ④$

When B-C junction becomes forward biased,

REVERSE CURRENT, $I_R = I_{CS}\left[\exp\left(\frac{qV_{BC}}{KT}\right)-1\right]$ $\rightarrow ⑤$

Substitute ④and ⑤ in ②,

$$I_C = \square_F I_{ES}\left(\exp\left(\frac{qV_{BE}}{KT}\right)-1\right) - I_{CS}\left(\exp\left(\frac{qV_{BC}}{KT}\right)-1\right) \qquad \rightarrow ⑥$$

Similar to② ,

Emitter current can be written as :

$$I_E = \square_R I_R - I_F \qquad \rightarrow ⑦$$

substitute ④and ⑤ in ⑦

$$\boxed{I_E = \square_R I_{CS}\left(\left[\exp\left(\frac{qV_{BC}}{KT}\right)-1\right]\right) - I_{ES}\left(\exp\left(\frac{qV_{BE}}{KT}\right)-1\right)} \qquad \rightarrow ⑧$$

By reciprocity relation,

$$\square_F I_{ES} = \square_R I_{CS} \qquad \rightarrow ⑨$$

* In saturation mode, BE and BC junctions are forward biased$\Rightarrow$ V_{BE}>0and V_{BC}>0

$$V_{CE}(sat) = V_{BE} - V_{BC} \qquad \rightarrow ⑩$$

Substitute⑧ in①

$$I_B + I_C = -\left(\square_R I_{CS}\left[\exp\left(\frac{qV_{BC}}{KT}\right)-1\right] - I_{ES}\left[\exp\left(\frac{qV_{BE}}{KT}\right)-1\right]\right)$$

$$-(I_B \square I_C) = \square_R I_{CS}\left[\exp\left(\frac{qV_{BC}}{KT}\right)-1\right] - I_{ES}\left[\exp\left(\frac{qV_{BE}}{KT}\right)-1\right]$$

$$V_{CE}(sat) = V_{BE} - V_{BC} = V_t \ln\left(\left[\frac{I_c(1-\square_R) + I_B}{(\square_F I_B - (1-\square_F) I_C)}\right]\frac{I_{CS}}{I_{ES}}\right)$$

$$\frac{I_{CS}}{I_{ES}} \approx \frac{\square_F}{\square_R}$$

$$V_{CE}(sat) = V_t \ln\left(\frac{I_C(1-\alpha_R) + I_B\ \alpha_F}{(\alpha_F I_B - (1-\alpha_F) I_C\ \alpha_R}\right)$$

X

2.9 GUMMEL POON MODEL

* This model is used if there is non uniform doping concentration in base. Electron current density in base of npn transistor,

$$J_n = q\mu_n n(x)E + qD_n \frac{dn(x)}{dx} \qquad \rightarrow ①$$

Electric field, $$E = V_T \frac{1}{p(x)} \frac{dp(x)}{dx}$$

$$E = \frac{KT}{q} \frac{1}{p(x)} \frac{dp(x)}{dx} \qquad \rightarrow ②$$

where p(x)→ majority carrier hole concentration in base

Substitute ②in①

$$J_n = q\mu_n n(x) \frac{KT}{q} \frac{1}{p(x)} \frac{dp(x)}{dx} + qD_n \frac{dn(x)}{dx} \qquad \rightarrow ③$$

By Einstein's relation,

$$J_n = \frac{qD_n}{p(x)}\left[n(x)\frac{dp(x)}{dx} + p(x)\frac{dn(x)}{dx}\right] \qquad \left(\because \mu_n \frac{KT}{q} = D_n\right)$$

$$J_n = \frac{qD_n}{p(x)} \frac{d(p_n)}{dx} \qquad \rightarrow ④$$

④can be rewritten as

$$\frac{J_n p(x)}{qD_n} = \frac{d(p_n)}{dx} \qquad \rightarrow ⑤$$

Integrating ⑤,

$$\frac{J_n}{qD_n}\int_0^{x_B} p(x)dx = \int_o^{x_B} \frac{dp_n(x)}{dx}dx$$

$$= p(x_B)n(x_B) - p(0)n(0) \qquad \rightarrow ⑥$$

We can assume B-E junction is forward biased and B-C junction is reverse biased

$$n(0) = n_{B0}\exp(V_{BE}/V_t)$$

$$n(x_B) = 0$$

$$n_{B0}p = n_i^2$$

$$\therefore ⑥ \Rightarrow J_n = \frac{-qD_n n_i^2 \exp(V_{BE}/V_t)}{\int_0^{x_B} p(x)dx} \qquad \rightarrow ⑦$$

* Integral in denominator →Total majority carrier charge in base →Base Gummel number (Q_B)

$$\text{Similarly } J_p = \frac{-qD_p n_i^2 \exp(V_{BE}/V_t)}{\int_o^{x_E} n(x')dx'}$$

* Integral in denominator → Total majoritycarrier charge in emitter → Emitter Gummel Number (Q_E)

2.9.1 EARLY EFFECT AND HIGH - LEVEL INJECTION:

* When CB voltage changes $\Rightarrow$ Neutral base width changes $\Rightarrow$ Base Gummel number Q_B changes $\Rightarrow$ Electron density - a function of CB voltage. This is called **Base width modulation or Early effect.**

* When B-E Voltage becomes very large, high level injection is applied$\Rightarrow$ Total hole concentration in base increases

$\Rightarrow$ Base Gummel number Q_B changes

$\Rightarrow$ Electron current density J_n changes.

This is called **high level injection.**

x

2.10 HYBRID - PI MODEL

$\rightarrow$ Small signal equivalent circuit of BJT using small - signal admittance parameters of pn junction.

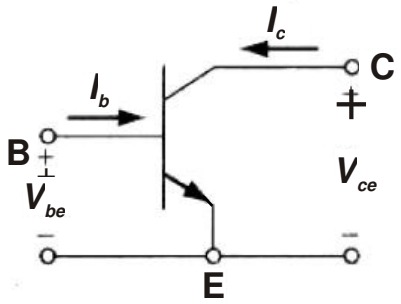


Fig 2.33 COMMON EMITTER npn BJT

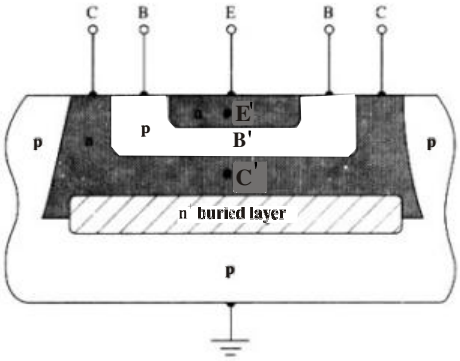
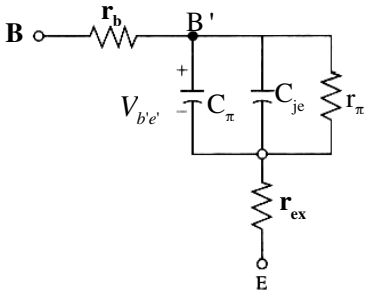


Fig 2.34 npn BIPOLAR TRANSISTOR FOR HYBRID - PI MODEL

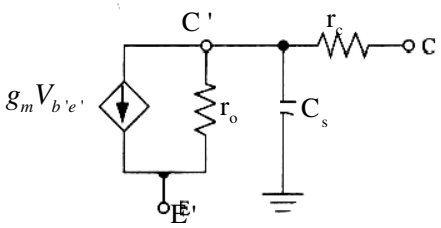
* C,B,E terminals → external connections to transistor

C ' ,B ' ,E ' terminals → idealized internal connections to transistor.



$V_{b'e'}$

Fig 2.35 a) Hybrid -PI Equivalent circuit Between Base and Emitter



b) Hybrid -PI Equivalent Circuit Between Collector and Emitter

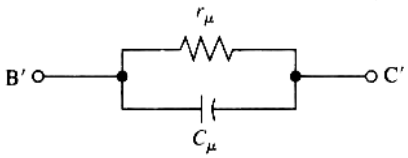


Fig 2.35 (c) Hybrid - PI Equivalent circuit between Base and Collector

* In Fig. 2.35 (a), r_b →series resistance in base between external base terminal B and internal base region B '.

* B ' - E ' junction is forward biased

  $C_{\square}$ → Junction diffusion capacitance

  $r_{\square}$ → Junction diffusion resistance

  $C_{\square} = C_d$

  $r_{\square} = r_d$

* $C_{\square}$ and $r_{\square}$ is parallel to junction capacitance C_{je}

* r_{ex} →series resistance between external emitter terminal E and internal emitter region E' .

* In Fig 2.35(b), r_c →series resistance between external collector terminal C and internal collector region C '.

  C_S → junction capacitance of reverse biased Collector - substrate junction.

$g_m V_{b'e'}$ →Collector current controlled by internal base emitter voltage.

$r_0 = \frac{1}{g_0} \rightarrow$ due to early effect

where g_0 →output conductance

* In Fig 2.35 (c), $C_{\square}$ = reverse biased junction capacitance

  $r_{\square}$ = reverse biased diffusion resistance.

C □ << C □

Miller capacitance → Equivalent capacitance between B ' and E ' due to C □ and feedback effect.

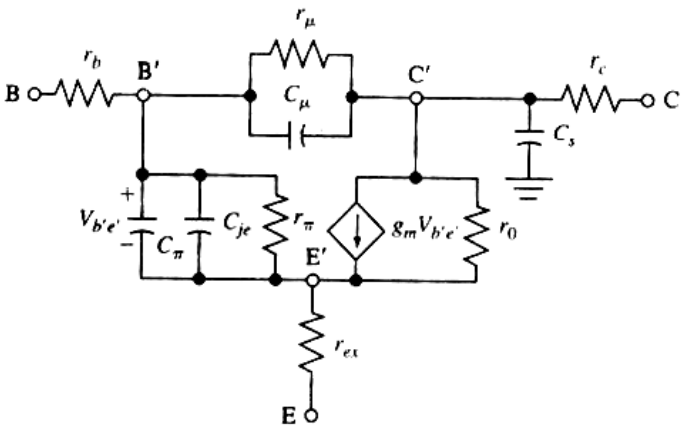


Fig 2.36 HYBRID - PI EQUIVALENT CIRCUIT

2.10.1 HYBRID - PI MODEL PARAMETERS IN TERMS OF h-PARAMETERS

1) TRANSISTOR TRANSCONDUCTANCE, g_m :

$$g_m = \frac{\square_0 I_E}{V_T}$$

$$\boxed{g_m \simeq \frac{I_C}{V_T}}$$

→ Transconductance is directly proportional to collector current and inversely proportional to Volt equivalent temperature.

2) INPUT CONDUCTANCE g_{be} :

Input resistance $r_{be} = \frac{h_{fe}}{g_m}$

$$= \frac{h_{fe}}{(I_C / V_T)} = \frac{h_{fe} V_T}{I_C}$$

$$r_{b'e} = \frac{h_{fe}}{g_m}$$

Input conductance $\boxed{g_{b'e} = \frac{g_m}{h_{fe}}}$

3) **FEEDBACK CONDUCTANCE** $g_{b'c}$ **:**

$$r_{b'c} = h_{re} r_{b'e}$$

$$\Rightarrow \boxed{g_{b'c} = h_{re} g_{b'e}}$$

4) BASE SPREADING RESISTANCE ($r_{bb'}$ **)**

$$\boxed{r_{bb'} = h_{ie} - r_{b'e}}$$

We know that

input resistance $r_{b'e} = \frac{h_{fe}}{g_m}$

$$= \frac{h_{fe}}{I_C / V_T} = \frac{h_{fe} V_T}{I_C}$$

$$\boxed{r_{bb'} = h_{ie} - \frac{h_{fe} V_T}{I_C}}$$

5) OUTPUT CONDUCTANCE (g_{ce})

$$h_{oe} = \frac{I_C}{V_{ce}}$$

$$= \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} \square g_m h_{re}$$

$$h_{oe} = g_{ce} + g_{b'c} + g_m h_{re}$$

$$= g_{ce} + g_{b'c} + g_{b'e} h_{fe} \quad h_{re}$$

$$(\because g_{b'e} = \frac{g_m}{h_{fe}})$$

$$h_{oe} = g_{ce} \square g_{b'c} \square g_{b'e} \quad h_{fe} \frac{g_{b'c}}{g_{b'e}}$$

$$(\because g_{b'c} = h_{re} g_{b'e})$$

$$= g_{ce} + g_{b'c} + h_{fe} g_{b'c}$$

$$= g_{ce} + g_{b'c}(1 + h_{fe})$$

$$\boxed{g_{ce} = h_{oe} - (1 + h_{fe}) g_{b'c}}$$

x

2.11 MULTI - EMITTER TRANSISTOR

INTRODUCTION:

→ Specialized BJT used at input of TTL NAND logic gates.

→ Input signals are applied to emitters

→ Collector current stops flowing only if all emitters are driven by LOGIC HIGH VOLTAGE.

→ Replace diodes of DTL and allows reduction of switching time and power dissipation.

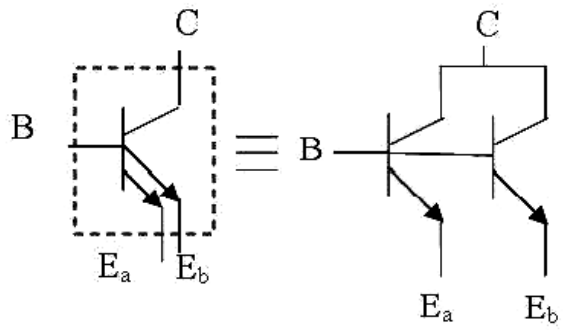


Fig 2.37 SYMBOL OF MULTI EMITTER TRANSISTOR

STRUCTURE:

* Multi emitter transistor consists of a wafer of semiconductor material having discrete emitter regions surrounded by base region.

* Base electrode consists of grid of solder connected to base region.

* A separate button of solder is connected to each emitter region.

* Emitter electrode consists of metal plate connected to each solder buttons and spaced from base electrode.

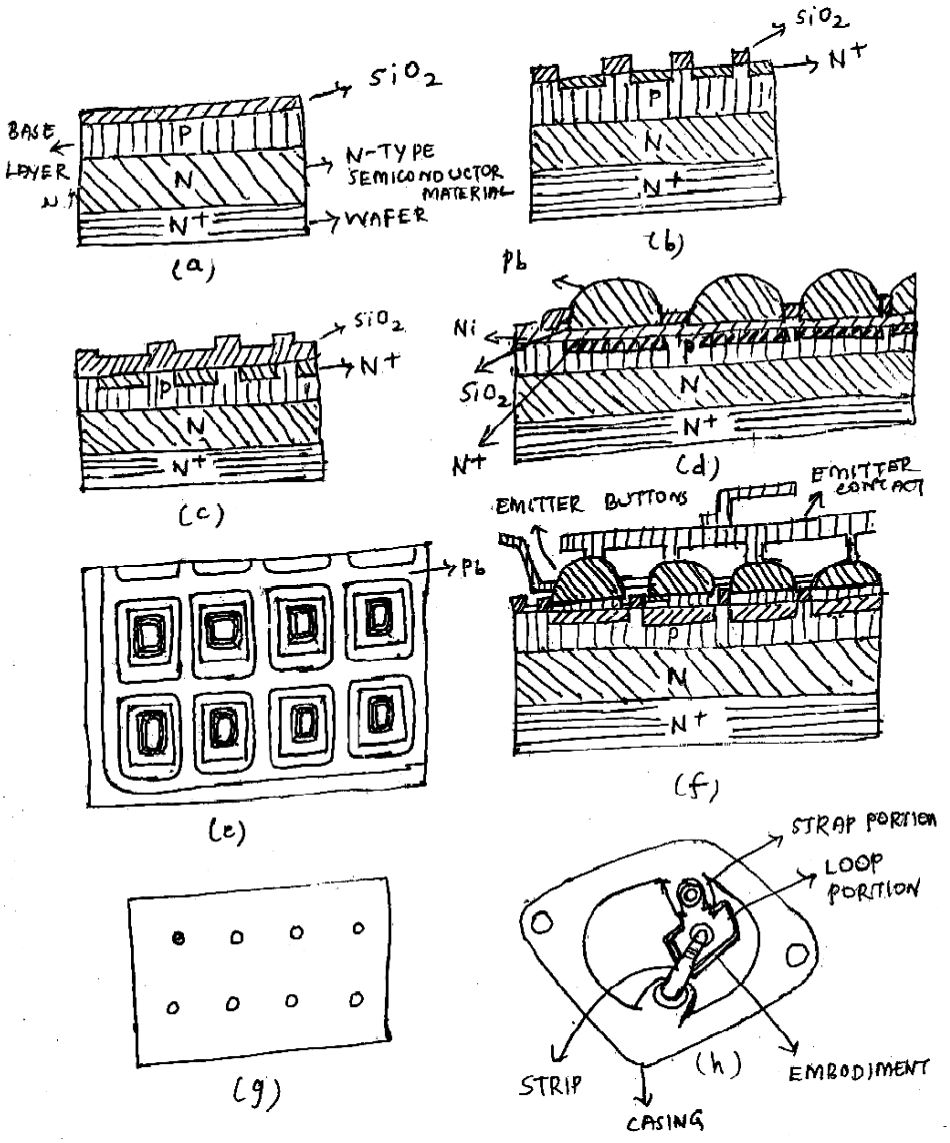


Fig 2.38 STRUCTURES OF MET

* Body of material consists of wafer of crystalline semiconductor material and N type semiconductor material.

* **Wafer** → Mono−crystalline silicon which is heavily doped with donor impurity (Phosphorus)to give N^+ conductivity.

* Epitaxial layer of N type silicon is deposited on wafer surface by a technique called "**SEMICONDUCTOR ART**"

* The layer is formed by passing mixture of hydrogen and silicon chloride over heated wafer.

* Base layer is formed in collector layer by diffusing impurity through collector layer surface through diffusion technique called as "**TRANSISTOR ART**".

* Base layer (P layer) is diffused in N layer to form PN junction. (**Figure (a)**)

* Electrically insulating coating is deposited on diffused base layer by **"SEMI CONDUCTOR ART**". Insulating coating consists of Silicon dioxide which is formed by thermal oxidation of Base layer.

* In figure (b), Openings are etched in insulated coating with etchant using photolithographic technique known as **SEMI CONDUCTOR ART.** Here photoresist coating is applied to oxide coating which is exposed to pattern of light to harden selected areas. Remaining areas are removed by solvent.

* Emitter regions are diffused in Base layer by heating base layer in ambient including N type impurity (**PHOSPHORUS PENTOXIDE**) (**FIGURE (b)**)

* Silicon dioxide coating is combined with insulating coating. Insulating coating is thicker in base region and thinner in emitter regions.(**Figure (c**))

* Silicon dioxide insulating coating is etched using **photolithographic masking** and **Etching techniques** to provide separate openings over each emitter regions. Communicating grooves are formed outside the openings.

* Major surface exposed by openings and grooves are coated by evaporation or plating with metal (Nickel)by **electroless plating** to produce thin nickel coating over exposed portions of major surface.(**Figure (d)**)

* Coating is exposed to molten solder by **dipping** and separate button of lead is formed over coating on emitter regions. Metallic base contact is also formed over nickel coating in each of the grooves.(**Figure(e)**)

* All emitter regions are connected. Emitter contact of metal (copper)is disposed over base contact and in contact with emitter buttons.

* Emitter contact is electrically connected to each of emitter buttons by heating transistor structure and emitter contact to a temperature at which emitter buttons fuse to emitter contact.(**Figure(f)**)

* A strip of metal (copper) consists of square loop portion connected to strap portion.

* Embodiment of transistor is mounted in casing of metal.

* Casing is used as heat sink and protection mechanism.

* N^+ Silicon wafer is soldered to casing. Strip is connected to one side of casing and insulated by electrical insulator.

* External lead (not shown) is soldered to strip for external circuit connections. Christo Ananth et al. [4] discussed about PN junction diode, Current equations, Diffusion and drift current densities, forward and reverse bias characteristics and Switching Characteristics of Semiconductor Diodes.

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[2] Christo Ananth, Vivek.T, Selvakumar.S., Sakthi Kannan.S., Sankara Narayanan.D, "Impulse Noise Removal using Improved Particle Swarm Optimization", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 3, Issue 4, April 2014,pp 366-370

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