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Design of Three Phase Seven Level Diode Clamped Multilevel Inverter

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Abstract - Multilevel inverters have become more popular over the years in high power electric applications without use of a transformer and with promise of less disturbance and reduced harmonic distortion. This work proposes three phase Seven level Diode Clamped Multilevel Inverter (DCMLI) to simulate various modulating techniques for induction motor load. These Pulse Width Modulation (PWM) techniques include Carrier Overlapping (CO) strategy, Variable Frequency (VF) strategy, Phase Shift (PSPWM) strategy and Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy and Alternate Phase Opposition Disposition (APOD) strategy. The Total Harmonic Distortion (THD), VRMS (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK. It is observed that PODPWM method provides output with relatively low distortion and COPWM is found to perform better since it provides relatively higher fundamental RMS output voltage for Induction Motor (IM) load

I.INTRODUCTION

Custom power devices are introduced in the distribution system to deal with various power quality problems faced by industrial and commercial customers due to increase in sensitive loads such as computer and adjustable speed drives and use of programmable logic control in the industrial process [1]-[3]. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of

the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected [4].

II. MULTI LEVEL INVERTER

The Multi-Level inverter has drawn a tremendous interest in power industry. They present an important in reactive power compensation. It may be either to produce a high power, high voltage inverter with Multi level inverter. Increasing the number of voltage level without requiring higher rating of individual levels can increase the power rating. As the number of voltage level increases the harmonic content decreases,
The concept of multilevel Inverter has been introduced since 1975.

The term *Multi-Level* began with the three levels Inverter. Subsequently, several multilevel Inverter topologies have been developed. However, the basic concept of a multilevel Inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources [7-9].

The commutation of the power switches aggregate these multiple dc sources to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only on the rating of the dc voltage sources to which they are connected. Consider a three phase inverter system with DC input voltage. Series connected capacitors constitute the energy tank of the inverter [5-6]. Each capacitor has the same voltage which is given by,

Em = (Voltage input Vdc)/ (m-1)

Where m denotes the number of levels, the term m denotes the number of nodes to which the inverter can be accessible

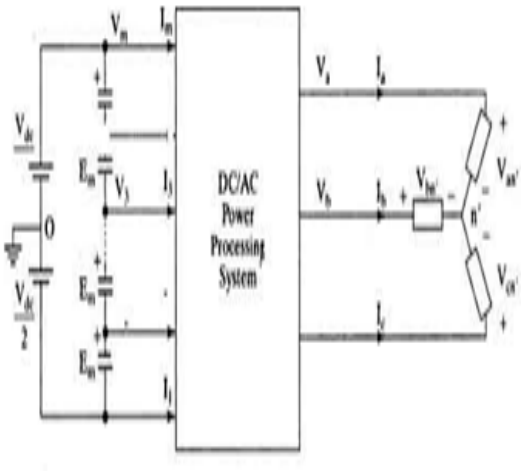

Fig 1: Multi Level Inverter with Series Connected Capacitors

III. DIODE CLAMPED MULTI LEVEL INVERTER

Multilevel VSC are the attractive technology for the medium voltage application, which includes power quality and power conditioning applications in the distribution system. A three-phase six level diode-clamped inverter is shown in Fig. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is *V*dc, and the voltage stress across each switching device is limited to *V*dc through the clamping diodes. Table lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage *V*0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require the other complementary switch to be turned off.

For a six-level inverter, a set of five switches should be on at any given time. The line voltage *V*ab consists of a phase-leg "a" voltage and a phase-leg "b" voltage. The resulting line voltage is a 11-level staircase waveform. This means that an *m*-level diode-clamped inverter has an *m*-level output phase voltage and a (2*m* − 1)-level output line voltage. Although each active switching device is required to block only a voltage level of *V*dc, the clamping diodes require different ratings for reverse voltage blocking. Using phase *a* of Fig as an example, when all the lower switches Sa_1 through Sa_5 are turned on, D4 must block four voltage levels, or 4*V*dc. Similarly, D3 must block 3*V*dc, D2 must block 2*V*dc, and D1 must block *V*dc. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, Dn will require *n* diodes in series; consequently, the number of diodes required for each phase would be (*m* − 1) × (*m* − 2).Thus, the number of

blocking diodes is quadratically related to the number of levels in a diode-clamped converter.

One application of the multilevel diode-clamped inverter is an interface between a high-voltage dc transmission line and an ac transmission line .Another application would be a variable speed drive for high-power medium-voltage (2.4–13.8 kV) motors as proposed .Several authors have proposed for the diode-clamped converter that static var compensation is an additional function

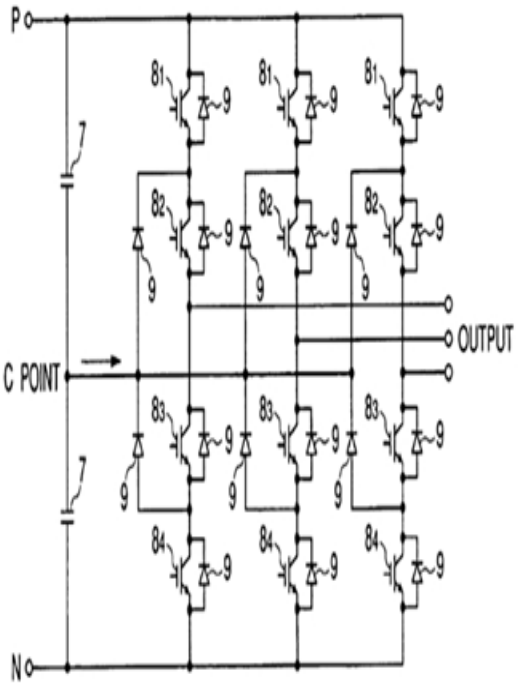

Fig 2: Approximated Diode Clamped Inverter

IV. IMPROVED DIODE CLAMPED INVERTER

The power rating of the parallel inverter will now be considered. The power transferred for voltage declines to less than 50% of nominal is predominantly real power, the parallel inverter would have to have an extraordinarily high rating if the conditioner were designed to compensate for such large voltage sags, just like the series inverter. However, unlike the series inverter, the dominant factor in determining the power rating of the parallel inverter is the load power factor if the conditioner is designed to compensate for only marginal voltage sags as shown in Fig. If the design of the universal power conditioner is to compensate for voltage sags to less than 50% of nominal voltage. If the design of the conditioner is for marginal voltage sags (to 70% of nominal voltage) and the MUPC will be applied to a customer load that has a power factor of less than 0.9, then the following equation is more suited for calculating the current rating of the parallel inverter's active devices

One common design for the parallel inverter in a universal power conditioner is for the inverter to have a

current rating equal to that of the rated load current

V.CHARACTERISTICS OF DIODE CLAMPEDMULTI-LEVEL INVERTER

The multilevel inverter performance operation is compared from the phase disposition strategy (PDPWM)

The rules for Phase disposition strategy for a multilevel inverter are

1. The converter is switched to + Vdc/2 when the sine wave is greater than both upper carrier.
2. The converter is switched to + Vdc/4 when the sine wave is greater than first upper carrier.
3. The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier
4. The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier.
5. The converter is switched to - Vdc/2 when the sine wave is less than both lower carriers.

The following formula is applicable to sub harmonic PWM strategy i.e. PD, POD and APOD The frequency modulation index mf = fc/fm The Amplitude modulation index ma = 2Am/ (m-1) Ac where fc – Frequency of the carrier signal fm – Frequency of the reference signal Am –Amplitude of the reference signal Ac – Amplitude of the carrier signal m – number of levels.

VI. SIMULATION RESULTS

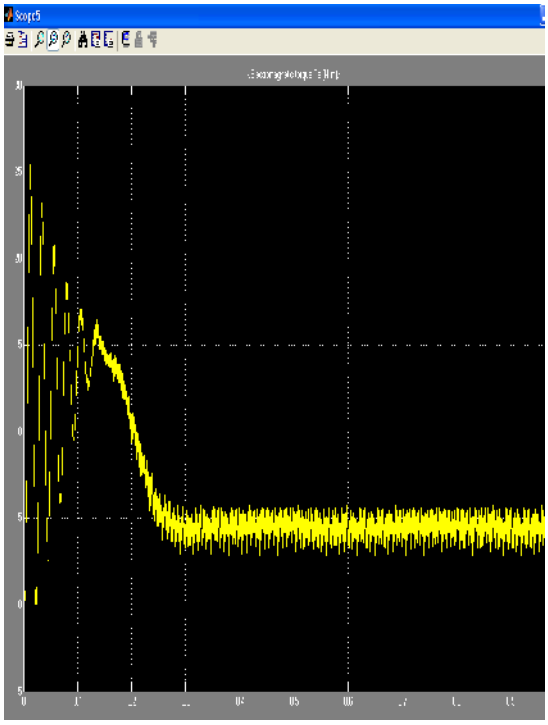

Fig 3: Torque vs Rotor angle

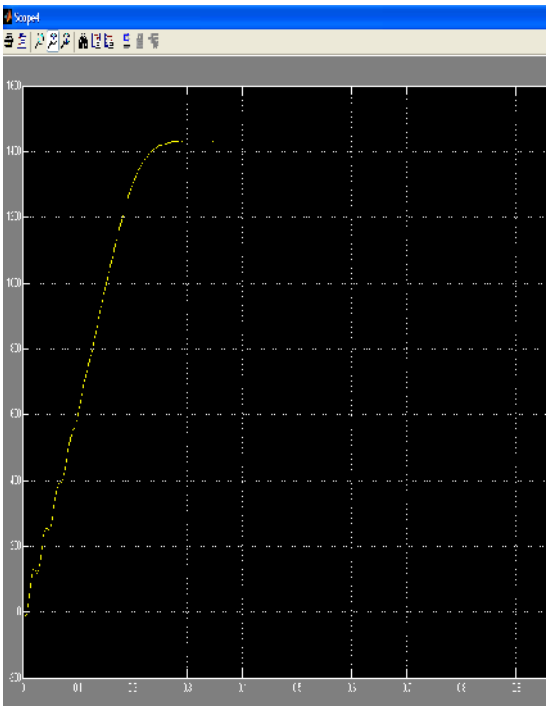

Fig 4: Speed vs Rotor Angle

VII. CONCLUSION

The above work proposes three phase Seven level Diode Clamped Multilevel Inverter (DCMLI) to simulate various modulating techniques for induction motor load. These Pulse Width Modulation (PWM) techniques include Carrier Overlapping (CO) strategy, Variable Frequency (VF) strategy, Phase Shift (PSPWM) strategy and Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy and Alternate Phase Opposition Disposition (APOD) strategy. Thus the Total Harmonic Distortion (THD), VRMS (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices.

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