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Low power clock distribution using a current pulsed global clockflip-flop

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***Abstract*--This paper describes, a new technique for clock distribution it uses current pulse. In previous method active mode and standby mode clock is enable. So power consumption is increased. By using low power clock distribution using a current pulsed global clocked flip-flop the active mode only enable D, the standby mode clock is disabled. It reduced power consumption. It uses one to many clock distribution networks. They achieve statistical power reduction by eliminating redundant transition and internal nodes. Theseflip-flops also have negative setup time. Current mode pulsed flip-flop with low power enable is combined with a current mode transmitter. Current mode clocked distribution network is lower average power compared to voltage mode clock.**

Keywords: Clockdistribution network, currentmode, flip flop,buffer, register block

I. Introduction

The portable electronic device has long battery life. The low power design hascritical in asynchronous application specific integrated circuits and system on chips. The system-on-chip design is integrating hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. It consists of the clock distribution network and sequential elements (flip-flop and latches), is one of the most power consuming components in a VLSI systems. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. Technology scaling reduces transistor and local interconnect delay and increasing the global interconnect delay.

A number of different clocking strategies can be used for implementing such systems, along with several different types of storage elements such as flip flop and latches. Current mode logic was an attractive high speed signaling scheme. Current mode consumes significant static power to offer the high speed. The static power dominates the dynamic power consumption in current mode schemes. In the paper, we present the current mode CDN and a new current mode pulsed D-flip flop where the clock input is a current mode receiver and the data input and active low enable output.

II. Overview of existing current mode signaling scheme:

The current mode signaling scheme, the transmitter utilizes a current mode input signal to transmit a current with minimal current swing into an interconnect. The receiver converts current to current providing a low swing output current for active mode not in a standby mode.

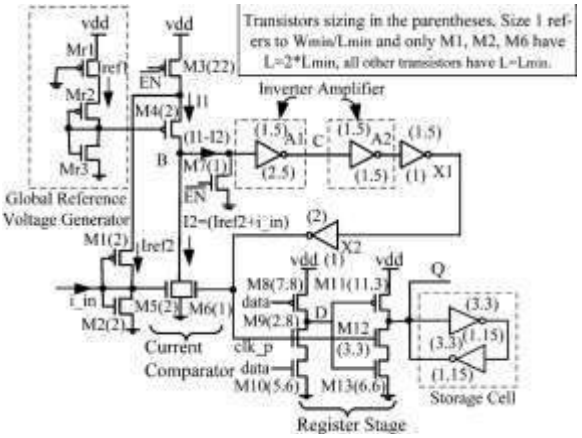

Fig1. The existing CMPFFE uses current-comparator and feedback connection to generate a voltage pulse that triggers a register stage to store data in the Storage cell.

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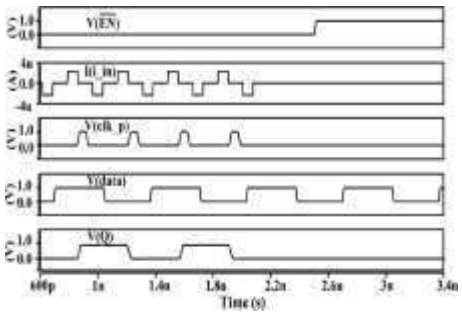

Fig2.Simulation waveforms confirm the internal current-to-voltage Pulse Generation (clk_p) that triggers input data capture.

III. Current mode global clocking pulsed flip flop with enable:

The proposed current mode global pulsed D Flip-flop with enable. It has D input signal. It uses an input comparator stage, buffer, register block. the current comparator stage compares the push pull current with a reference current. The current mode receiver logic consume low amount of static power even when the circuits are in standby mode and active mode With the decrease in feature size of CMOS integrated circuits(IC), interconnect design has become a primary issue in high speed ICs. Interconnect design is most often used to increase circuit speed; however, the interconnect also affects the power dissipated by a circuit . Clock networks can dissipate a large portion of the total power dissipated within a synchronous IC in which consists of the clock distributionnetwork and timing elements (flip-flops and latches),is one of the most power consuming components in a VLSIsystem .[6] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

It accounts for 30% to 60% of the total powerdissipation in a system. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed.Voltage scaling is the most effective way to decrease power consumption, since power is proportional to the square of the voltage. However, voltage scaling is associated with threshold voltage scaling which can cause the leakage to increase exponentially.

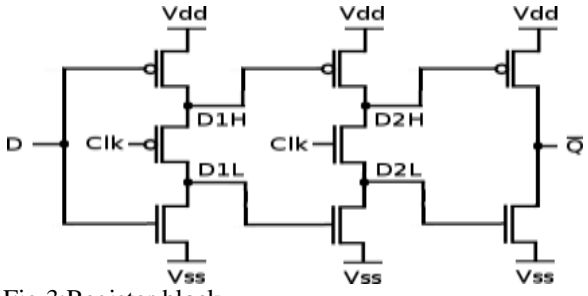

Fig 3:Register block

The Current comparator stage compares the input push pullcurrent with a reference current and conditionally amplifiesthe clock to a full-swing voltage pulse that triggers the data to latch at the register stage. The feedback pulsed FF is in stark contrast to the previous CM schemes which utilized expensive Rx circuits and buffers to drive the final FFs.

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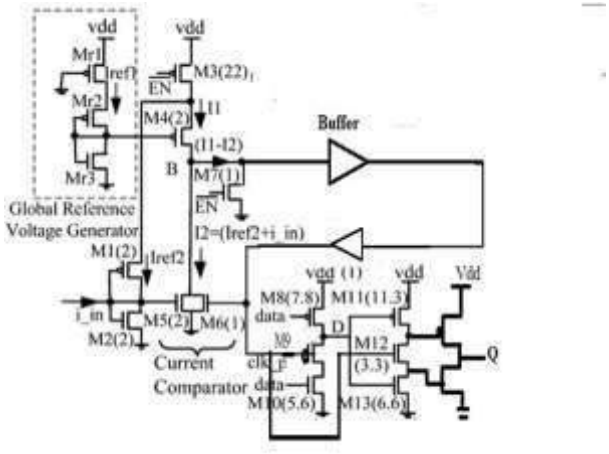

Fig3. The proposed CMPFFE with global clock uses current-comparator and feedback connection to generate a voltage pulse that triggers a register block.

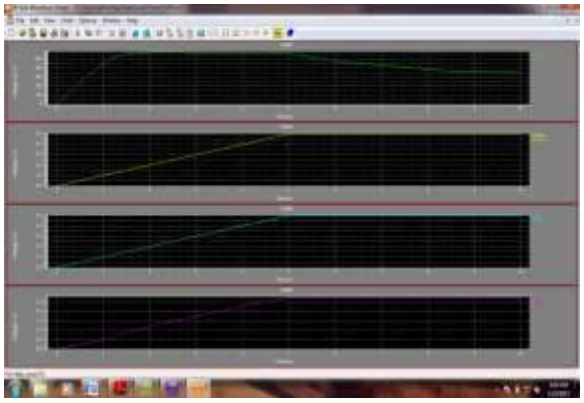

Fig4.Simulation waveforms for current to current pulse Generation (clk-p) that triggers input data capture.

The choice of push-pull current enables a simple Tx circuit while maintaining a constant bias voltage on the CDN interconnect.The CMPFFE with global clock pulse is only sensitive to unidirectional push current which provides the positive edge trigger operation of the Flip flop. This design is easily modified using a complementary current comparator in to negative clock edge FF using the pullcurrent.it disables the static current I1 in stand-by mode is low. The internal node B is decoupled with stand-by mode, the additional transistor M7 is ground the internal clock node and prevent any unintentionallatching of input data. Transistor M7 is disabled during normal operation. Adding an extra OFF transistor will introduce a stacking effect in the CC. which in turn will reduce the leakage current in M4. The peak CMPFFE leakage current is smaller than the peak switchingcurrent in active mode. the global routing requires extra metal resources. Since the proposed current mode require buffers in the current distribution network, it is easy to globally route .In the input stage, the reference voltage generator Mr2 and Mr3 creates a reference current is mirrored by M4 and generates current I1.the M1–M2 pair creates the FF reference current which is combined with the input current this current is then mirrored by M3.It is possible to use a local or global reference voltage generator for the input gate voltage of M4. Using a global reference can increase the robustness by reducing transistor mismatch between FFs. Hence, we used a global reference voltage generator that distributed across the whole chip,

when we integrate the CMPFFE with the current mode current distribution network globally. This also saves five invertor gate per FF and reduces static power .

we used a simple buffer circuit. A buffer amplifier is one of that provides electrical impedence transformation from one circuit to another with the aim of the signal source beingunaffected by (buffered from)what ever currents(or voltages for a current buffer0that the load may produce.an electronic circuits whose primary function is to connect a high impedence source to a low impedence load with outsignificantattenuation or distortion of the signal.hence the output voltage of a buffer replicates the input voltage without loading the source.buffers are generally applied in analog systems to minimize loss of signal strength due to excessiveof output nodes.current buffer is a circuit that is used transfer current from a low input impedence circuit to a circuit having high input impedence,the current buffer circuit connected in between the two circuits prevents the second circuit from loading the first circuit.

The features of an ideal current buffers are:

- Infinite input impedance
- Zero output impedance.
- Perfect linearity, regardless of signal of signal amplitudes.
- Instant output response, regardless of the speed of the input signal.

A current buffer with unity gain(B=1)is called a unity gain current buffer or current follower.

IV. Conclusion:

In this paper, we presented the current mode flip flop and its usage in a fully CM CDN. The proposed CMPFFE is 90% faster. the current mode global clock pulsed flip flop enables power reduction. the active mode only have enable the clock signal and the stand by mode the clock signal are disabled.

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