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ANALYSIS OF FUZZY LOGIC CONTROLLER FOR TRANSFORMER-LESS VOLTAGE QUADRUPLER BOOST CONVERTER

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Abstract: **The work focused on the development of a transformer-less adjustable voltage Quadrupler DC Boost Converter with Fuzzy Logic Controller to enhance high-voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle. The projected converter cannot only achieve high step-up voltage gain with reduced number of component. It also reduces the voltage stress of both active switches and diodes. This will allow to choose lower voltage rating of IGBTs and diodes to reduce both switching and conduction losses. Closed loop Fuzzy Logic Controller is used to achieve the desired output voltage. The operation principle and steady analysis as well as a comparison with other recent existing high step-up topologies are presented. Experimental and simulation and results are presented to demonstrate the effectiveness of the proposed converter**.

Keywords: Voltage quadrupler, Boost Converter, Buck-Boost converter, Fuzzy logic controller.

I. INTRODUCTION

For Global energy shortage a renewable energy sources such as solar cells and fuel cells are increasingly widely used. However, owing to the inherent low voltage characteristic of these sources, a high step-up dc converter is essential as a pre stage of the corresponding power conditioner. The conventional boost and buck–boost converters, due to the degradation in the overall efficiency, as the duty ratio approaches unity. Moreover, the extreme duty ratio not only induces very large voltage spikes and increases conduction losses but also induces severe diode reverse-recovery problem. A simple isolated structure with a high step-up voltage gain is dc-dc fly back converter, because of the leakage inductance of the transformer converter will suffer a high voltage stress. Some energy-regeneration techniques have been proposed to clamp the voltage stress on the active switch and to recycle the leakage inductance. To achieve a high step-up gain by increasing the turn's ratio of the transformers some isolated voltage type converters are existing such as the phase shifted full bridge converters. Unfortunately, the large amount of input current ripple will reduce the maximum output power and cut down the usage life of input electrolytic capacitor. More input electrolytic capacitors are required to suppress the large input current ripple. In additional to that, the circuit efficiency is degraded because of high output diode voltage stress than the output voltage in the high-output-voltage applications.

Other isolated current-type converters are existing such as the active-clamp dual-boost converters and the active-clamp full bridge boost converters, can realize high efficiency and high step-up conversion. Because of many extra power components causes to increase the cost. In order to reduce system cost and to improve system efficiency a non-isolated dc/dc converter is a suitable solution. The switched capacitor-based converters proposed to improve the conversion efficiency and achieve large voltage conversion ratio. Numeral aspects are arises because of the usage of conventional switched capacitor are suffering high transient current and large conditional losses. Some converter topologies were presented based on a switched capacitor cell concept in which a soft switched scheme was used to reduce the switching loss & electromagnetic interference Some interleaved high step-up converters with coupled inductors are introduced to derive more compact circuit structure. To achieve higher voltage conversion ratio and further reduce voltage stress on the switch and diode, the high step-up ratio converter and the ultrahigh step-up converter have been proposed. These converters can provide large step-up voltage conversion ratios. Unfortunately, the voltage stress of diodes in those converters remains rather high. In this paper, a transformer-less adaptable voltage quadrupler topology is proposed. It integrates two-phase interleaved boost converter to realize a high voltage gain and maintain the advantage of an automatic current sharing capability simultaneously. Furthermore, the voltage stress of active switches and diodes in the proposed converter can be greatly reduced to enhance overall conversion efficiency.

II. EXISTING SYSTEM

The conventional boost and buck-boost converters, due to the degradation in the overall efficiency as the duty ratio approaches unity.

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Besides, the extreme duty ratio not only induces very large spikes and increases conduction losses but also induces severe diode reverse – recovery problem. Active switch of high step-up voltage gain will suffer a voltage stress due to leakage inductance of the transformer. Output diode voltage stress is much higher than the output voltage, which will degrade the circuit efficiency in the high output voltage applications. [5] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.Cost is increased because extra power components and isolated sensors or feedback controllers are required.

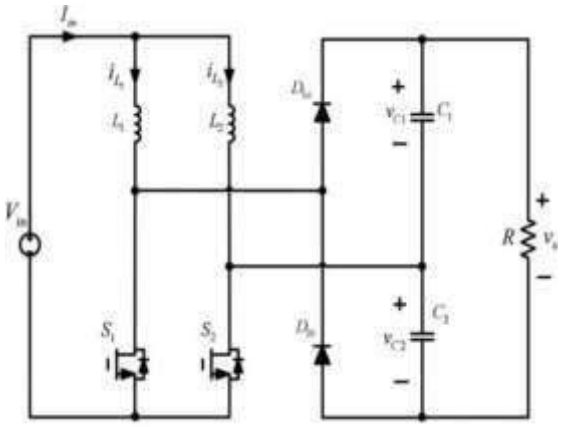

Fig. 1 Block diagram of Existing System.

DRAWBACKS OF EXISTING SYSTEM

- Active switch suffer high voltage stress due to leakage induction of Transformer.
- To achieve High step up gain by increasing the turns ratio of Transformer.
- Very large voltage spikes increases the conduction losses but also induces severe diode reverse recovery problem.
- Input current ripple is relatively high.
- Higher input current ripple will reduce the maximum output power and shorten the usage life of input
- Electrolytic capacitor.
- Higher output voltage stress will degrade the circuit efficiency.
- Cost is high due to extra power components.

III. PROPOSED SYSTEM

With Global energy shortage and strong environmental movements, renewable or clean energy sources such as solar cells and fuel cells are increasingly valued worldwide. However due to the inherent low voltage characteristic of these sources, A Transformer – less DC Boost converter with low switch voltage stress to enhance efficiency has been proposed with the help of Fuzzy Logic Controller.

DESIGN PARAMETERS

- Power =200W
- V_{IN}=12V
- I_{IN}=16A
- V_{OUT}=200V
- I_{OUT} =1A
- Gain of Converter = 4/1-D

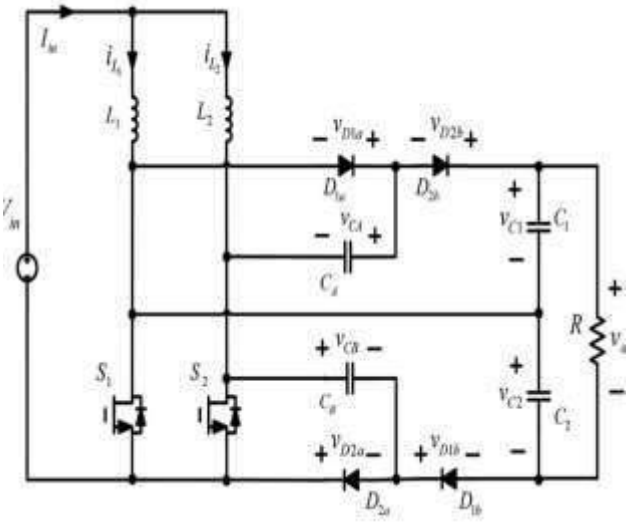

Fig. 2 Circuit Diagram of the proposed converter

DUTY CYCLE CALCULATION

Gain of converter = 4/1-D
D is duty ratio
V_{OUT} / V_{IN} =4/1-D
1-D = 4/ (V_{OUT} / V_{IN})
D = 1- 4/ (V_{OUT} / V_{IN})
D = 1- 4/ (200 / 12)
D = 0.77

INDUCTOR VALUE

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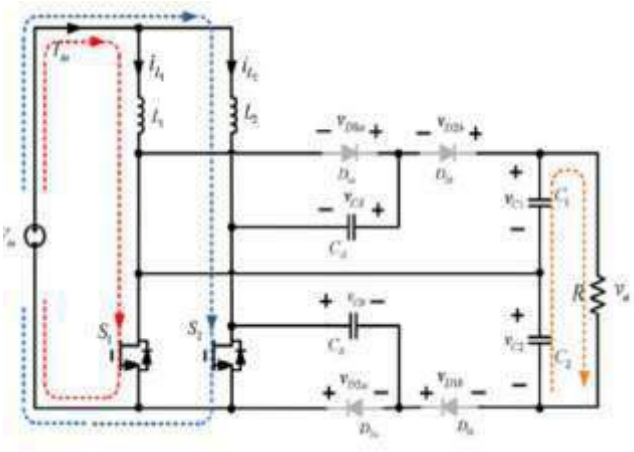

Fig. 3 Mode 1

In above mode (Mode 1), when the IGBT is on, voltage across the inductor will be equal the voltage of the battery.

$V_{IN} = V_L = 12$

For an inductor voltage current basic relation is

$V_L = L * dI / dt$

Then, $L = V_L * dt / dI$

$L = V_{IN} * dt / dI$

Here dt = Duty Cycle / Frequency

Assume that operating frequency of the switch (IGBT here) =40 kHz

and dI IS the ripple current of inductor

Since 2 inductors of same value will take equal current from battery

$I_L = I_{IN}/2$

$I_L = 16A/2$

$I_L = 8A$

Assume that inductor ripple current = 20% of inductor current

$dI = 20\% * I_L$

$dI = 20\% * 8A$

$dI = 1.6A$

$L = V_{IN} * dt / dI$

$L = V_{IN} * D / (F * di)$

$L = 12V * 0.77 / (40000 Hz * 1.6A)$

$L = 144uH$

OUTPUT CAPACITOR C_1 AND C_2 VALUE

In Above Mode (Mode 1), Load Consumes Power From C1 And C2 Which Is In Series.

$I_{C1} = I_{C2} = P_{OUT} / V_{OUT}$

$I_{C1} = I_{C2} = 200W / 200V$

$I_{C1} = I_{C2} = 1A$

For a capacitor voltage current basic relation is

$I = C * dV / dt$

$C = I * dt / dV$

dV is output ripple voltage. Assume that output ripple voltage is about 0.08% of output voltage

$dV = 0.08\% * 100V$

$dV = 0.08 V$

$C = I * dt / dV$

We have dt = duty ratio/frequency

$C = I * D / (F * dV)$

$C = 1A * 0.77 / (40000 Hz * 0.08 V)$

$C = 240 uF = 220uF$ (Standard value)

CAPACITOR C_a and C_b VALUE

In above mode (mode2), at load side current through C_1 capacitor will be sum of load current and i_{ca}

$I_{c1} = i_{ca} + i_{out}$

$C_1 * d_{vC1} / dt = i_{ca} + i_{out}$

$C_1 = 250uf$

$dv = 0.08\% * 100v$

dv = 0.08 v

We have dt = duty ratio/frequency

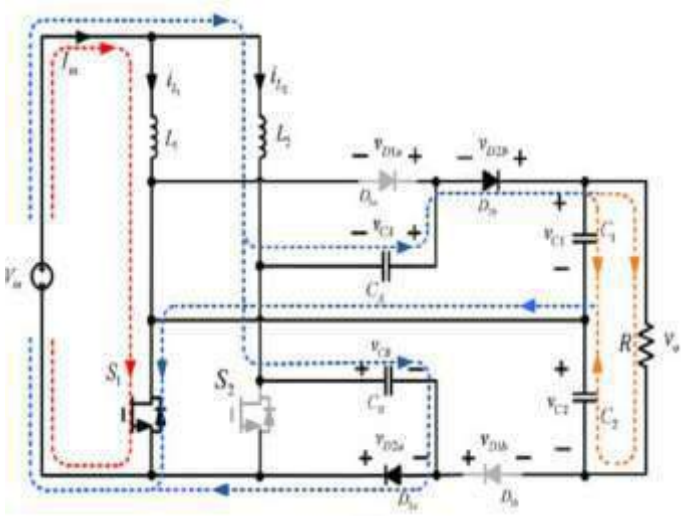

Fig. 4 Mode 2

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$C_1 * d_{vC1} * F / D = i_{ca} + i_{out}$
$250uF * 0.08V * 40000Hz/0.77 = i_{ca} + 1A$
$I_{ca} = (250uF * 0.08V * 40000Hz/0.77) - 1A$
$I_{ca} = 1.04 - 1A$
$I_{ca} = 0.04A$
For a capacitor voltage current basic relation is
$I_{ca} = c_a * dv_a / dt$
$C_a = i_{ca} * dt / dv$

dv_a is output ripple voltage. Assume that output ripple voltage is about 0.08% of output voltage.

C_a is charged by inductor $V_{IN} / 1-D$

$V_a = V_{IN} / 1-D$

$V_a = 12 / 1-0.77$

$V_a = 52$

$dv = 0.08\% * 52v$

$dv = 0.0416$ v

$C = i_{ca} * dt / dv$

We have dt = duty ratio/frequency

$C = i_{ca} * d / (f * dv)$

$C = 0.04$ a* 0.77/ (40000 Hz* 0.0416 v)

C = 18.50 uf = 22uf (standard value)

IV. OPERATION OF THE PROPOSED CONVERTER

For convenient reference, the two-phase interleaved boost converter with parallel-input series-output connection is first shown in Fig 6.2. The proposed converter topology is basically derived from a two-phase interleaved boost converter. Comparing Fig 3 with Fig 6.2, one can see that two more capacitors and two more diodes are added so that during the energy transfer period partial inductor stored energy is stored in one capacitor and partial inductor stored energy together with the other capacitor store energy is transferred to the output to achieve much higher voltage gain. However, the proposed voltage gain is twice that of the interleaved two-phase boost converter. Also, the voltage stress of both active switches and diodes are much lower than the latter. Furthermore, as will be obvious latter, the proposed converter possesses automatic uniform current sharing capability without adding extra circuitry or complex control methods. The detailed operating principle can be illustrated as follows.

The proposed converter topology, like any existing high step-up dc converter, possesses the drawback of existence of pulsating output period. Furthermore, as the main objective is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous conduction mode (CCM); hence, the steady state analysis is made only for this case. However, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. In addition, only with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit. On the other hand, when duty cycle is smaller than 0.5, the converter does not possess the automatic current sharing capability any more, and the current-sharing control between each phases should be taken into an account in this condition.
In order to simplify the circuit analysis of the proposed converter, some assumes are made as follows:
1) All components are ideal components
2) The capacitors are sufficiently large, such that the voltages across them can be considered as constant approximately.
3) The system is under steady state and is operating in CCM and with duty ratio being greater than 0.5 for high step-up. Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with a 180◦ phase shift as well as some key operating waveforms are shown below.

MODE 1 ($T0 \leq T < T1$):

For mode 1, switches S1 and S2 are turned ON, $D_{1a}, D_{1b}, D_{2a}, D_{2b}$ are all OFF. The corresponding equivalent circuit is shown in Fig 4.6.1. From Fig 4.6.1, it is seen that both i_{L1} and i_{L2} are increasing to store energy in L_1 and L_2, respectively. The voltages across diodes D_{1a} and D2a are clamped to capacitor voltage V_{CA} and V_{CB}, respectively, and the voltages across the diodes D1b and D2b are clamped to V_{C2} minus V_{CB} and V_{C1} minus V_{CA}, respectively. Also, the load power is supplied from capacitors C_1 and C_2.

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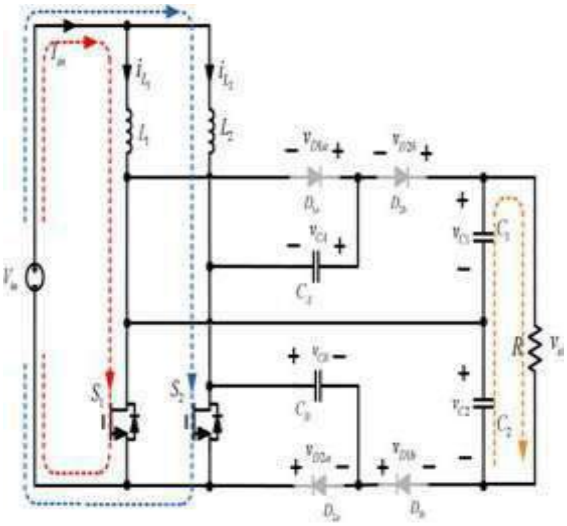

Fig.5 Mode I & III Operation.

MODE 2 (T1 ≤ T < T2) :

For this operation mode, switch *S*1 remains conducting and *S*2 is turned OFF. Diodes D_{2a} and D_{2b} become conducting. The corresponding equivalent circuit is shown in figure below. It is seen from that part of stored. Energy in inductor L_2 as well as the stored energy of C_A is now released to output capacitor C_1 and load. Meanwhile, part of stored energy in inductor L_2 is stored in C_B. In this mode, capacitor voltage V_{C1} is equal to V_{CB} plus V_{CA}. Thus, i_{L1} still increases continuously and i_{L2} decreases linearly. The corresponding state equations are given as follows:

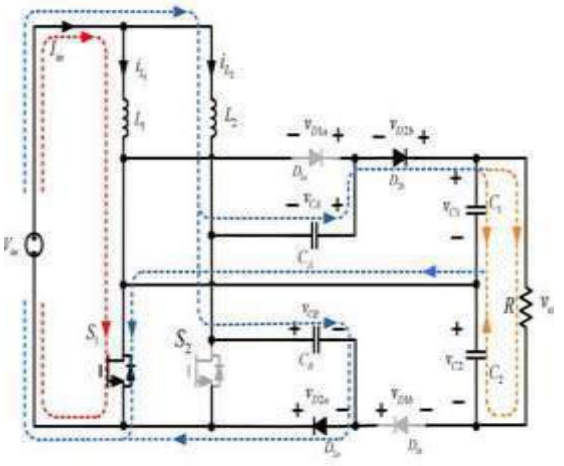

Fig. 6Mode II Operation.

MODE 3 (T2 ≤ T < T3):

For this operation mode, as can be observed, both S_1 and S_2 are turned ON. The corresponding equivalent circuit turns out to be the same.

MODE 4 (T3 ≤ T < T4):

For this operation mode, switch S_2 remains conducting and S_1 is turned OFF. Diodes D_{1a} and D_{1b} become conducting. The corresponding equivalent circuit, it is seen from that the part of stored energy in inductor L_1 as well as the stored energy of C_B is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 is stored in C_A. In this mode, the output capacitor voltage V_{C2} is equal to V_{CB} plus V_{CA}. Thus, i_{L2} still increases continuously and i_{L1} decreases linearly.

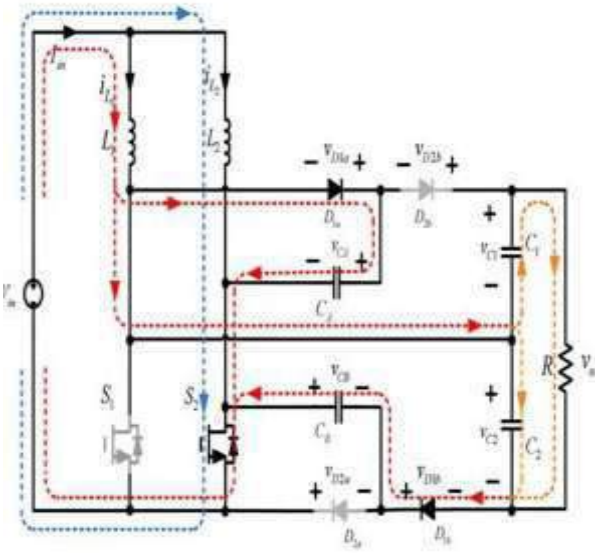

Fig. 7 Mode IV Operation.

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V. SIMULATION RESULTS

SIMULATION BLOCK DIAGRAM

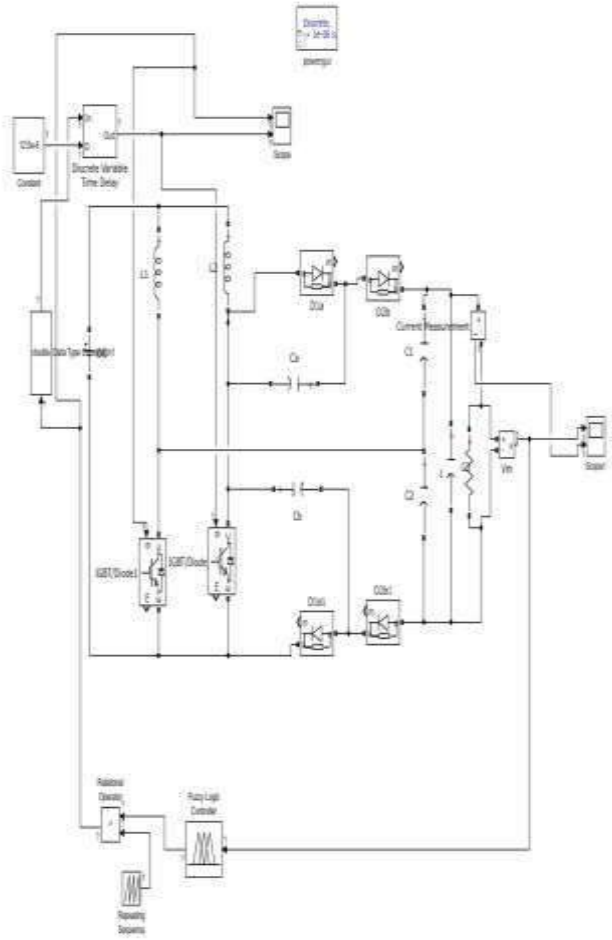

Fig. 8 Simulation Block Diagram

INPUT WAVEFORM

Fig. 9 Input waveform

PWM GENERATION FOR THE PROPOSED CONVERTER

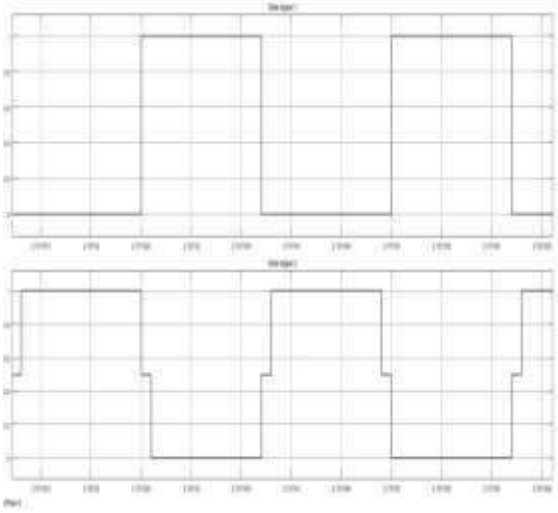

Fig. 10 PWM Generation For The Proposed Converter

OUTPUT VOLTAGE WAVEFORM

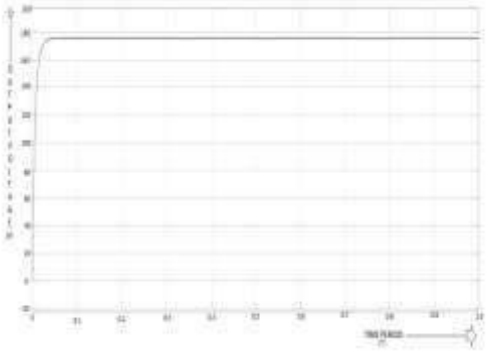

Fig 11 Output Voltage Waveform from the converter

OUTPUT CURRENT

Fig 12 Output current Waveform from the converter

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VI. EXPERIMENTAL RESULT

A Transformer-less Adaptable Voltage Quadrupler DC Boost converter with Fuzzy Logic Controller prototype is built to verify the circuit operation.
The circuit parameters are:

- Input voltage: 12 DC
- Output voltage: 192V DC
- Switching frequency, 100 kHz.

Voltage Gain

V_{in}= 12V

$$Vo = Vc1 + Vc2 = \frac{4}{1-??} * Vin = \frac{4}{1-0.75} * 12 = 192V$$

$$Vc1 = Vca + Vcb = \frac{2}{1-??} * Vin = \frac{2}{1-0.75} * 12 = 96V$$

$$Vc2 = Vca + Vcb = \frac{2}{1-??} * Vin = \frac{2}{1-0.75} * 12 = 96V$$

VII. CONCLUSION

A Transformer-less DC Boost converter with Fuzzy Logic Controller to enhance efficiency with high voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration and is derived from a two-phase interleaved boost converter for providing a much higher voltage gain without adopting an extreme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain but also reduce the voltage stress of both active switches and diodes. This will allow one to choose lower voltage rating JFETs and diodes to reduce both switching and conduction losses. In addition, due to the charge balance of the blocking capacitor, the converter features automatic uniform current sharing characteristic of the two interleaved phases for voltage boosting mode without adding any well as a comparison with other recent existing high step-up topologies are presented. Finally, a 200-W rating prototype with 12-V input and 192-V output is constructed for verifying the validity of the proposed converter. It is seen that the resulting experimental results indeed agree very close and show great agreement with the simulation results. Therefore, the proposed converter is very suitable for applications requiring high step-up voltage gain.

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