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High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator

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Abstract:

A high-speed, low-power, and highly reliable frequency multiplier is proposed for a delay-locked loop-based clock generator to generate a multiplied clock with a high frequency and wide frequency range. The proposed edge combiner achieves a high-speed and highly reliable operation using a hierarchical structure and an overlap canceller. The proposed frequency multiplier minimizes the delay difference between positive-edge and negative-edge generation paths, which causes a deterministic jitter. Finally, a numerical analysis is performed to analyze and compare the performance of the proposed frequency multiplier with that of previous frequency multipliers. The proposed frequency multiplier is fabricated using a 0.13-μm CMOS process technology, and has the multiplication ratios of 1, 2, 4, 8, and 16, and an output range of 100 MHz–3.3 GHz. The frequency multiplier achieves power consumption to a frequency ratio of 2.9 μW/MHz.

Index Terms:

Clock generator, delay-locked loop (DLL), edge combiner, frequency multiplier.

I. INTRODUCTION

DYNAMIC voltage and frequency scaling (DVFS) is currently being used in nearly every system-on chip (SoC), because DVFS can efficiently lower the dynamic power consumption of the SoCs while maintaining the performance. DVFS, which detects the SoC workload and dynamically changes the supply voltage and frequency, requires a dc–dc converter and a clock generator. The clock generator is generally implemented using a phase-locked loop (PLL) to easily change the output clock frequency. However, PLLs have several weaknesses such as the difficulty of design, high-cost loop filters, and jitter accumulation. Delay-locked loops (DLLs) are a good substitute for PLLs, because they resolve the PLL weaknesses; however, because a DLL uses a delay line instead of an oscillator, its output clock frequency is always the same as its input clock frequency. Therefore, a DLL alone cannot be used as a clock generator. Several DLL-based clock generators have been proposed to solve this problem.

The DLL-based clock generator is composed of a DLL core and a frequency multiplier, and the frequency multiplier is generally divided into two blocks: 1) a pulse generator and 2) an edge combiner. In case that variable frequency multiplication is required, multiplication-ratio control logic is added. The DLL core generates multiphase clocks using a reference clock in the DLL core. The pulse generator generates the appropriate number of pulses from the multiphase clocks according to the multiplication-ratio control signal, and the edge combiner generates a multiplied clock using the selected pulses. In general, the maximum multiplication ratio of the frequency multiplier is half of the number of multiphase clocks. Because the frequency multiplier generates the multiplied clock by simply collecting the multiphase clocks, jitter accumulation does not occur. In addition, the frequency multiplier can easily change multiplication ratios. However, to increase the maximum multiplication ratio, the logic depth or output loading of the frequency multiplier must be increased. However, it severely degrades the maximum multiplied clock frequency. To solve the problems of the previous frequency multiplier, a novel frequency

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multiplier is proposed in this paper. A hierarchical structure and an overlap canceller are used for the proposed edge combiner. Owing to the proposed edge combiner, the proposed frequency multiplier can generate a higher frequency and wider frequency range multiplied clock with a lower power consumption per frequency ratio and higher reliability than previous frequency multipliers. Christo Ananth et al. [4] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced.The structures and problems of the previous frequency multipliers are described. The structure and the operation of the proposed frequency multiplier are described. Theoretical analyzes of the multiplied clock frequency of the previous and the proposed frequency multipliers. The measurement results are presented. Finally, the conclusion is drawn.

II. PREVIOUS FREQUENCY MULTIPLIERS

Frequency multipliers that perform better than most previous frequency multipliers. The frequency multiplier in is composed of a D-flip–flop-based pulse generator, a multiplication-ratio control logic, and a push–pull-stage based edge combiner. Owing to its simple edge-combiner structure, this frequency multiplier is suitable for high-frequency multiplied clock generation with low power and a small area. It can also guarantee a 50% duty cycle for its multiplied clock. However, because the output pulses of the pulse generator are generated consecutively [i.e., the kth pulse is generated directly following the ($k-1$) the pulse], the pulses might overlap owing to process variation or layout mismatch as they pass through the multiplication-ratio control logic; this could cause a short-circuit current to flow in the edge combiner, which in turn could lead to excessive power consumption or malfunction of the frequency multiplier. In addition, the output loading of the edge combiner rapidly increases with the multiplication ratio, because one pull-up pMOS (PU-P) and one pull-down nMOS (PD-N) are added to the output of the edge combiner whenever the maximum multiplication ratio increases by one. This frequency multiplier is composed of multiplication-ratio control logic, an AND-gate-based pulse generator, and a differential cascade voltage switch (SW) logic (DCVSL)-stage-based edge combiner.

The frequency Multiplier can generate the multiplied differential clocks with a small area penalty. As only one PD-N is added to each differential output of the edge combiner when the maximum multiplication ratio is increased by one, the output loading of the edge combiner increases slower than that of the edge Combiner. However, the PD-N should remain on till the positive and the negative edges of the multiplied differential clocks are generated by the edge combiner. In addition, when the PD-N is turned ON, the edge combiner uses a small-sized PU-P to prevent conflict between the PU-P and the PD-N. Because of these restrictions, the frequency multiplier may not be suitable for high-speed operation and cannot guarantee 50% duty cycle for the multiplied clock. Finally, interphase timing distortion may occur when the multiphase clocks pass through the multiplication-ratio control logic, which in turn can generate pulse overlapping similar to that experienced in the frequency multiplier in. The frequency multiplier has the same structure as, with the exception that its edge combiner is composed of a modified DCVSL stage and a push–pull stag. The modified DCVSL stage has SWs that turn the PU-P OFF when the PD-N is ON, preventing conflict between the PU-P and the PD-N. Therefore, a small-sized PU-P is no longer required; this property efficiently solves the slow operation problem of the DCVSL-stage-based edge combiner. In addition, by adopting a push–pull stage, 50% duty cycle can be guaranteed for the multiplied clock. Finally, as the modified DCVSL stage maintains the characteristics of a DCVSL structure, only one PD-N is added to each differential output of the modified DCVSL stage when the maximum multiplication ratio is increased by one, as in the edge combiner. However, the frequency multiplier still has some problems in common with the frequency multiplier, including reliability degradation owing to pulse overlapping.

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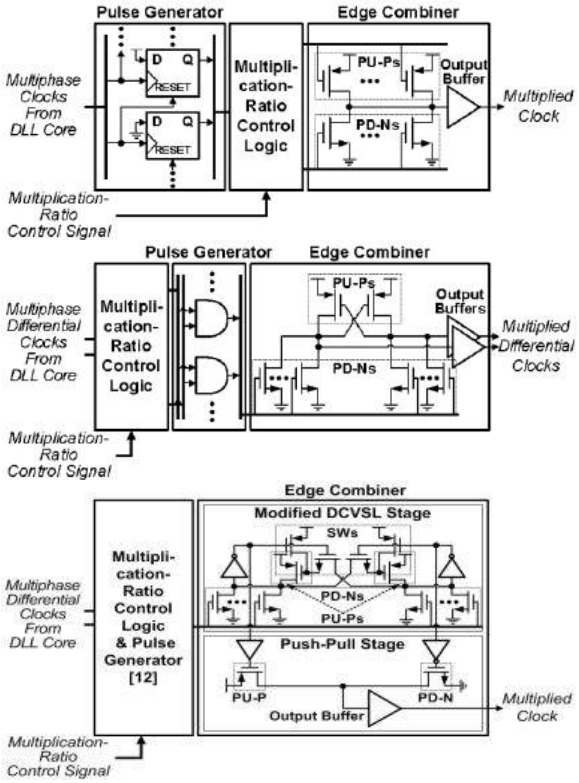

III. PROPOSED FREQUENCY MULTIPLIER

The proposed DLL-based clock generator is composed of a DLL core and the proposed frequency multiplier. To enhance the lock time, which is an important design parameter in the clock generator, a dual-edge-triggered phase-detector-based DLL core is adopted. Similar to previous frequency multipliers, the proposed frequency multiplier is also composed of a pulse generator, multiplication-ratio control logic, and an edge combiner. The dual-edge-triggered Phase-detector compares both the positive and the negative edges of CLKREF, DCK and CLKOUT, DCK, which are the duty cycle recovered clocks of CLKREF and CLKOUT using the duty-cycle keeper. The DLL is locked within 300 cycles in all process–voltage–temperature corners owing to the dual-edge detection characteristic, and generates 32-phase differential clocks (CLK0:32 and /CLK0:32*)*. Using the 32-phasedifferential clocks, the pulse generator makes pulses (PG0:31 and /PG0:31*)* for positive- and negative-edge generation. The multiplication-ratio control logic selects appropriate pulses from PG0:31 and /PG0:31 and generates MC*P* ,0:15 and MC*N*,0:15 according to the multiplication ratio control signal. Finally, the high-speed and highly reliable edge combiner (HSHR-EC) generates one multiplied clock (CLKMUL*)* using all the outputs of the multiplication ratio control logic. Since the number of multiphase is 32, the maximum multiplication ratio is 16. To solve the speed and the reliability issues of previous edge combiners, an HSHR-EC, which consists of a pre combining stage, overlap canceller, and push–pull stage is proposed. The two-step edge combiner, pre combining, and push–pull stage are used to enhance the maximum multiplied clock frequency. The overlap canceller is used to guarantee the stable operation of the frequency multiplier.

As the number of signals merged in the pre combining stage (*N*PRE*)* increases, the number of PU-Ps and PD-Ns required in the push–pull stage are reduced by a factor of *N*PRE. It might appear that, by increasing *N*PRE, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; however, because the logic depth and the number of NAND and NOR gates in the precombing stage are equal to log2*N*PRE and 32(1–1/*N*PRE*)*, respectively, a large *N*PRE causes the precombining stage to be vulnerable to process variation, which in turn could cause a large deterministic jitter. Thus, *N*PRE is limited to two, which corresponds to a logic depth of one in the HSHR-EC, and thus, the precombining stage can be simply realized using NAND and NOR gates. As is true for the frequency multipliers the proposed frequency multiplier may suffer from pulse overlapping owing to the multiplication-ratio control logic. To prevent this, an overlap canceller is inserted between the precombing and the push–pull stages. The overlap canceller consists of simple NAND and NOR gates. If the delay of PC*P,*0(PC*N,*0*)* generation path is less (more) than that of PC*N,*0 (PC*P,*0*)* generation path because of the process variations or layout mismatches, overlap between the high level of PC*P,*0 and the low level of PC*N,* 0 can be generated. The NAND gate with PC*P,* 0 and PC*N,* 0 inputs makes OC*P,*0 low only when both PC*P,*0and PC*N,* 0 are high.

This eliminates pulse overlapping. Similarly, if the delay of the PC*N,*0 (PC*P,*1*)* generation path is less (more) than that of PC*P,*1 (PC*N,*0*)* generation path due to process variations or layout mismatches, overlap can exist between the low level of PC*N,*0 and the high level of PC*P,*1. Because a NOR gate makes OC*N,* 0 high only when both PC*N,* 0 and PC*P,* 1 are low, pulse overlapping is eliminated. Thus, highly reliable operation of the frequency multiplier can be guaranteed. The proposed frequency multiplier can properly generate the high-frequency multiplied clock owing to the overlap canceller when 1000

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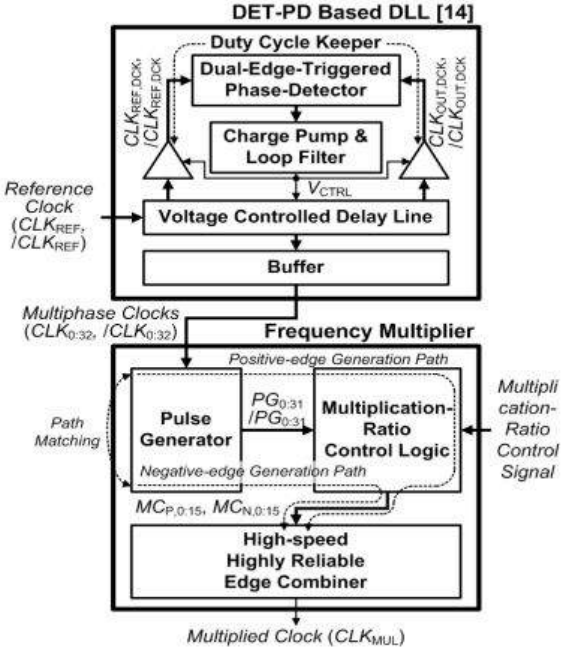
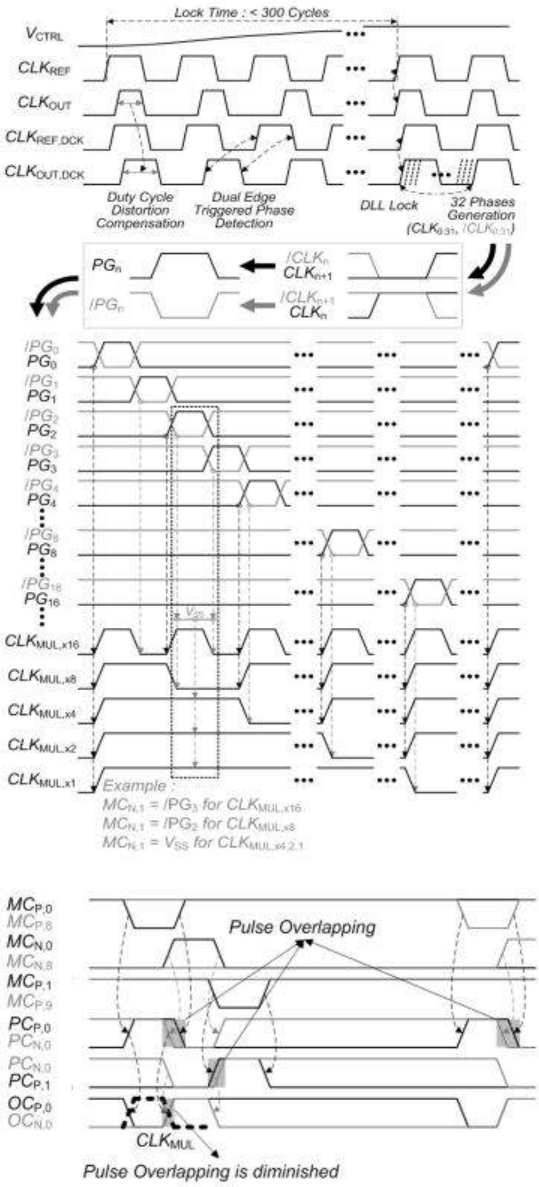
Monte Carlo simulations are performed. Delay mismatch between the positive- and negative-edge generation paths of the multiplied clock can generate Deterministic jitter, necessitating precise delay matching. These two structures have an optimized design to match the delay between the positive- and negative-edge generation paths of the multiplied clock. Owing to these pulse generator and multiplication-ratio control logic structures, the positive- and negative-edge generation paths of the multiplied clock have the same structures (two NAND gates, two NOR gates, one tristate inverter, and one inverter). Because both the paths have the same path logical effort, they can be designed to have the same delay, and thus, the deterministic jitter can be minimized.





CLOCK GENERATOR

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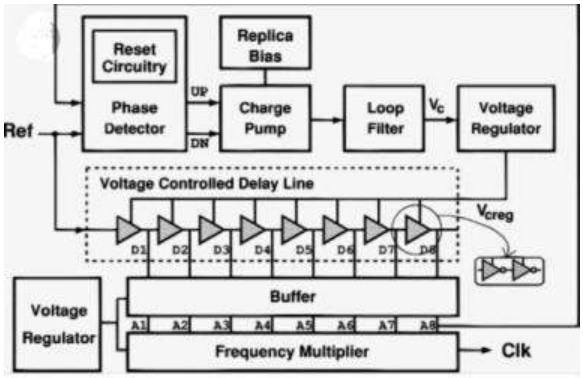
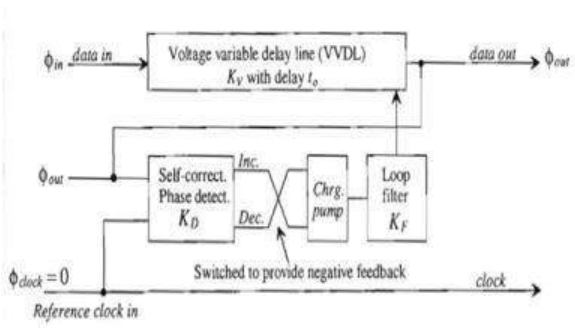


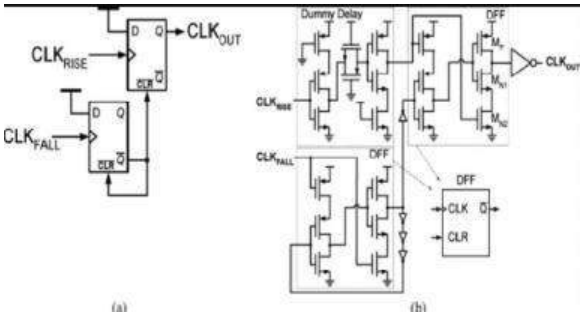
A clock generator produce timing singal for use in synchronizing a circuit's operation. The signal can range from a simple symmetrical square wave to more complex arrangements.

DELAY LOCKED LOOP



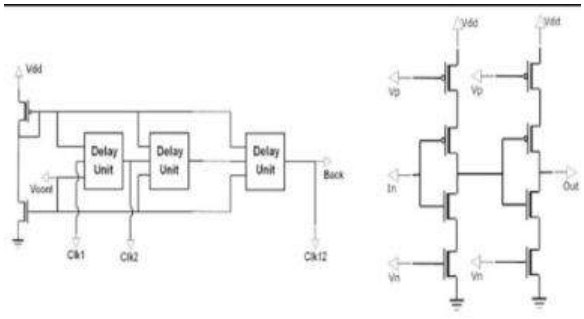
The delay locked loop is a variable delay line whose delay is locked to the duration of the period of a reference clock. A DLL can be used to change the phase of a clock signal, usually to enhance the clock rise-to-data output valid timing characteristics of IC.

EDGE COMBINER



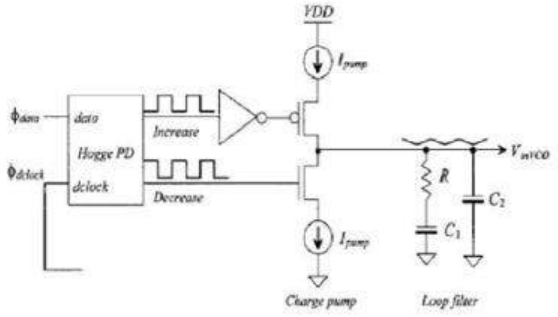
An edge combiner can combine the multiple clock phases and act as a programmable frequency multiplier useful in dynamic voltage.

FREQUENCY MULTIPLIER



A frequency multiplier generates on output signal whose output frequency is a harmonic of its input frequency.

CHARGE PUMP



A charge pump is used to provide a charge to a capacitive element on a voltage controlled delay line (voltage controlled delay line).Where in the charge is independent of a control voltage step cycle time of the DLL

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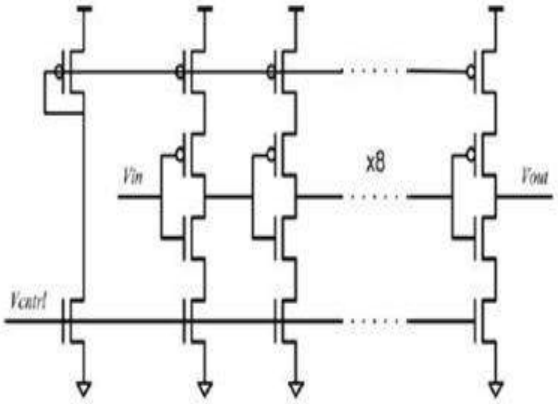
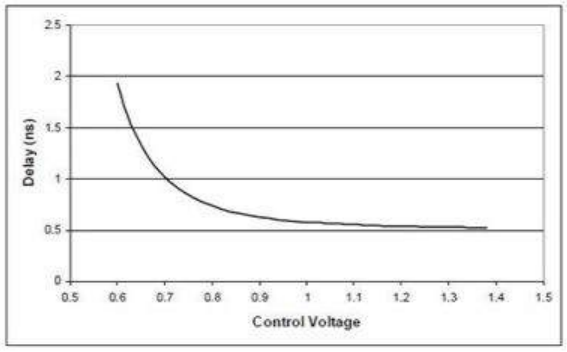
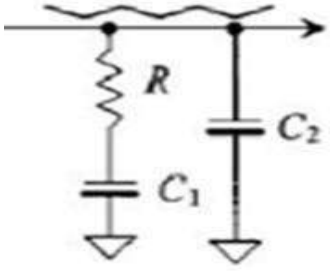




The function of Voltage Controlled Delay Line (VCDL) is to delay the reference signal so that there is no skew between the output clock and reference signal. The VCDL takes two inputs: a control voltage and a clock. The output is a clock of the same frequency as the input, but phase shifted by some amount proportional to the control voltage.

LOOP FILTER



Loop filter

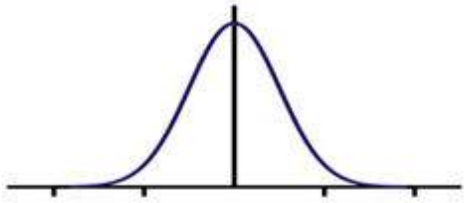


FIG: Shape of the impulse response of a typical Gaussian filter.

In electronics and signal processing, a Gaussian filter is a filter whose impulse response is a Gaussian function. Gaussian filters have the properties of having no overshoot to a step function input while minimizing the rise and fall time

IV. NUMERICAL ANALYSIS

The maximum multiplied clock frequency of the proposed frequency multiplier is compared with the previous frequency multipliers. Because it is determined by the edge-combiner structure, the edge combiners and the proposed HSHR-EC are analyzed using the Elmore delay model. First of all, the push–pull-stage-based edge combiner can be expressed as follows:

$$f_{\mathrm{MUL,MAX}} \propto \frac{1}{2t_{\mathrm{PE(NE)}}} = \frac{1}{2\frac{\beta}{k_P}\{\mathrm{MR_{MAX}}(1+k_P)+k_O\}R_N C_{j,N}}$$
$$\mathrm{ERR_{DUTY}} \propto t_{\mathrm{PE}} - t_{\mathrm{NE}} = \{\mathrm{MR_{MAX}}(1+k_P)+k_O\}\cdot\left(1-\frac{\beta}{k_P}\right)R_N C = 0 \quad (1)$$

Where t_{PE}(NE*)* is the time required for the positive (negative)- edge generation, *RN* is the ON-resistance of the PD-N, *Cj, N*is the junction capacitance of the PD-N, *C*OB is the gate capacitance of the output buffer, β is the mobility ratio (assuming that all MOSFETs have the same channel length) between the PU-P and the PD-N, *kP* and *kO* are, respectively, the normalized channel widths of the PU-P and the output buffer with respect to the channel width of the PD-N, *f*MUL ,MAXis the maximum multiplied clock frequency, and ERRDUTY is the duty-cycle error of the multiplied clock. In the push–pull stage- based edge combiner, *KP* is designed to be equal to β. Thus, t_{PE} equals *t*NE, and ERRDUTY is zero. Second, the DCVSL-stage-based edge combiner can be expressed as follows:

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$$f_{\mathrm{MUL,MAX}} \propto \frac{1}{2\left(1+\frac{\beta}{k_P}\right)\cdot(\mathrm{MR_{MAX}}+k_P+k_O)\,R_N C_{j,N}}$$
$$\mathrm{ERR_{DUTY}} \propto -\frac{\beta}{k_P}(\mathrm{MR_{MAX}}+k_P+k_O)\,R_N C_{j,N}. \quad (2)$$

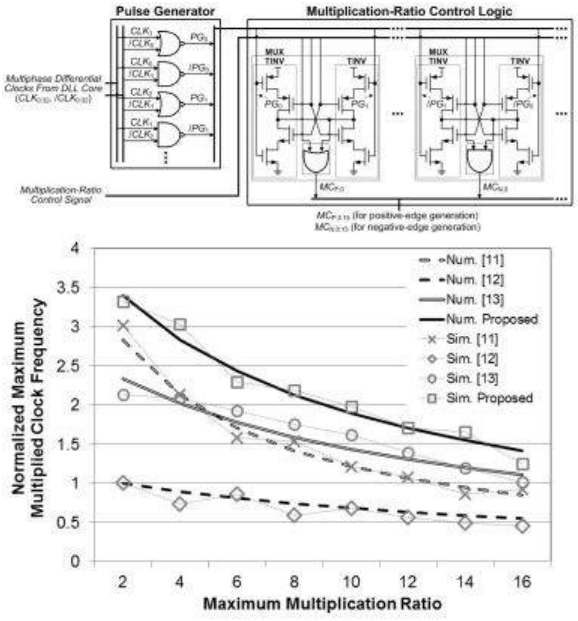
Since t_{PE} is always greater than tNE, fMUL, MAX is determined byt_{PE}, and ERRDUTY is always negative. Third, the edge combiner in [13] can be expressed as Follows:

$$f_{\mathrm{MUL,MAX}} \propto \frac{1}{2\left\{\left(1+\frac{\beta}{k_P}\right)\cdot(\mathrm{MR_{MAX}}+K_1)+\left(1+\frac{1}{k_{SN}}\right)\cdot K_2\right\}R_N C_{j,N}} \quad (3)$$
$$\text{where } K_1 = k_P + k_{SN} + k_I, K_2 = k_{SN} + k_{SP} + k_P + 2k_I$$
$$\mathrm{ERR_{DUTY}} \propto \{(1+k_P)+k_O\}\cdot\left(1-\frac{\beta}{k_P}\right)R_N C_{j,N} = 0$$

Where *k*SN *(k*SP*)* and *kI* are the normalized channel widths of then MOS (pMOS) SW and the output buffer with respect to the channel width of the PD-N, respectively. Since duty cycle is solely decided by the push–pull stage, ERRDUTY is zero, which is the same characteristic with the edge combiner. The HSHR-EC has similar properties to those of the edge combine. However, because the precombining stage in the HSHR-EC merges two signals into one, the self-loading of the push–pull stage (output loading of the push–pull stage except the loading induced by the output buffer) is halved. The maximum multiplied clock frequency of the HSHR-EC can be expressed as follows:

$$f_{\mathrm{MUL,MAX}} \propto \frac{1}{2\frac{\beta}{k_P}\{0.5\,\mathrm{MR_{MAX}}(1+k_P)+k_O\}R_N C_{j,N}}$$
$$\mathrm{ERR_{DUTY}} \propto \{0.5\mathrm{MR_{MAX}}(1+k_P)+k_O\} \times\left(1-\frac{\beta}{k_P}\right)R_N C_{j,N} = 0. \quad (4)$$

The numerical analysis and the simulation results for the normalized maximum multiplied clock frequency as a function of the maximum multiplication ratio; all frequency multipliers are designed and simulated using a 0.13-μm process technology. It is seen that the simulation results show a tendency similar to the numerical analysis. The normalized maximum multiplied clock frequencies of the frequency multipliers in and are less than those of the frequency multiplier, and the proposed frequency multiplier because of the structural problems. The frequency multiplier has the best performance among the previous frequency multipliers, because the modified DCVSL stage in its edge combiner has better features than that of the edge combiners, i.e., the driving strength of the PU-P and the PD-N in the edge combiner is the same as that of the push–pull-stage-based edge combiner, and the output loading is lower than that of the DCVSL-stage-based edge combiner. The proposed frequency multiplier shows the best performance owing to its HSHR-EC. By incorporating a precombining stage into the HSHR-EC, the proposed frequency multiplier can attain a maximum multiplied clock frequency that is nearly twice that of the frequency multiplier. While the modified DCVSL stage in the edge combiner in solves the weak PU-P usage problem of the DCVSL-stage-based edge combiner, it still has performance limitations owing to the structural characteristics of the DCVSL; namely, the positive edge can be generated only after the negative edge is generated. Thus, although the HSHR-EC has a greater output loading and the same PU-P and PD-N driving strengths as the modified DCVSL stage in the edge combiner, the proposed frequency multiplier can achieve a higher maximum multiplied clock frequency than the frequency multiplier.



V. MEASUREMENT RESULTS

The proposed frequency multiplier is implemented using a 0.13-μm CMOS process technology, and has a supply voltage of 1.2 V. Fig. 9 shows a chip micrograph of the proposed frequency multiplier and the DLL core used for the frequency multiplier measurement. The overall test chip occupies an active area of 0.037 mm2, and the proposed frequency multiplier has the multiplication

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ratios of 1, 2, 4, 8, and 16, and a maximum multiplied clock Frequency of 3.3 GHz. Because the minimum operating frequency of the DLL core is 100 MHz, the multiplied clock frequency has a range from 100MHz to 3.3 GHz. At 3.3 GHz, the frequency multiplier and the overall DLL-based clock generator consumed 9.6 and 24.7 mW, respectively. The detailed power breakdown for the proposed DLL-based clock generator at 3.3 GHz is presented. The output waveform and the jitter of the DLL-based clock generator measured in the worst case condition; the operating frequency of the measured multiplied clock is 3.3 GHz with the 206.25 MHz input reference clock, giving a multiplication factor of 16. The duty-cycle error of the multiplied clock is −0.9%–0.4%, and the rms and the peak-to-peak jitter are 1.85 and 13.6 ps, respectively. The performance variation of the proposed clock generator with regard to the multiplication ratio and the DLL reference clock. First of all, the power-frequency ratio increases as the multiplication ratio decreases, because the power consumption of the frequency multiplier almost linearly scales down with decreasing the multiplication ratio, but that of the DLL core is fixed.

The power-frequency ratio also increases as the DLL reference clock frequency decreases, because the power consumption of the DLL core does not scale down as much as the frequency multiplier due to static power consuming blocks such as charge pump and biasing circuits. Second, the jitter slightly decreases as the multiplication ratio decreases, because the jitter induced by the delay cell mismatch in Voltage Controlled Delay Line (VCDL) reduces. Instead, jitter is largely dependent on DLL reference clock frequency. Because the VCDL generates one period delay of DLL reference clock, the slope of the clocks in VCDL should be degraded at a low DLL reference clock frequency. Due to this characteristic, jitter increases at a low DLL reference clock frequency. Finally, the duty-cycle error decreases as the multiplication ratio and the DLL reference clock frequency decreases, because the duty-cycle error is deterministic. Thus, the duty-cycle error becomes the largest value at the highest multiplied output clock frequency. The performance summary and provides a comparison with the previous clock generators. Among the DLL with frequency multiplier architectures, the proposed frequency multiplier achieves the highest maximum multiplication ratio and the highest maximum multiplied clock frequency. In addition, it has a low (although not the lowest) power consumption to frequency ratio (power–frequency ratio in Table I), because the proposed frequency multiplier has a slightly more complex structure than that , which shows the lowest power consumption to frequency ratio and a slightly higher power consumption to frequency ratio.

However, because the proposed frequency multiplier achieves a higher multiplication ratio, the DLL core does not require a high operating frequency. Thus, the proposed clock generator (frequency multiplier with DLL core) achieves the lowest power consumption to frequency ratio among the DLL with frequency multiplier architectures. Because the proposed clock generator has the highest maximum multiplication ratio and the areas of the DLL core and the frequency multiplier are proportional to the maximum multiplication ratio, the area of the proposed clock generator is larger than that of previous DLL with frequency multiplier architectures. However, the normalized area of the proposed clock generator, which is the area divided by the product of the square of the process technology and the maximum multiplication ratio, is lower than that of other clock generators. To evaluate the proposed clock generator, a reputable figure of merit (FoM) for a PLL (FoM1 in Table I) is adopted. However, because FoM1 only concentrates on the aspect of performance, area and multiplication range, which are the most important design parameters for a clock generator, cannot be compared using FoM1. For example, if the maximum multiplication ratio increases, power and area penalties are inevitable, but this phenomenon cannot be explained using FoM1. Thus, the modified FoM based on FoM1 and normalized area (FoM2 in Table I) is suggested in this paper. The FoM2 is expressed as follows:

$$\mathrm{FoM2} = 10\log\left[\left(\frac{\mathrm{Jitter_{rms}}}{1\ \mathrm{s}}\right)^2 \cdot \frac{\mathrm{Power}}{1\ \mathrm{mW}} \cdot \frac{\mathrm{Area}}{\mathrm{process}^2 \cdot \mathrm{MR_{MAX}}}\right] \quad (5)$$

Where MRMAX is the maximum multiplication factor. Compared with DLL with frequency multiplier architectures, the proposed clock generator shows the superior performance according to both FoM1 and FoM2, as expected. Note that both the multiplying DLL and the PLL architecture superior performance than the proposed clock generator in FoM1. Even the area and the multiplication ratio are considered using FoM2, the multiplying DLL is still shows better performance than the proposed clock generator. This result is mainly due to the outstanding power consumption of the multiplying DLL and the PLL architecture. However, the DLL with frequency multiplier architecture has more chance to contribute

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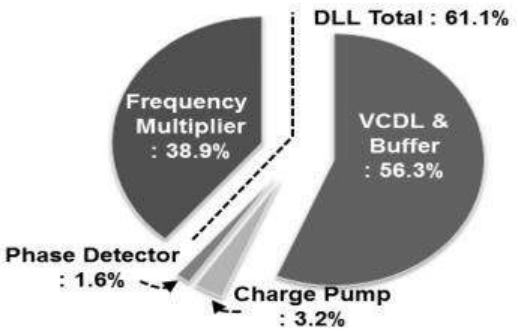
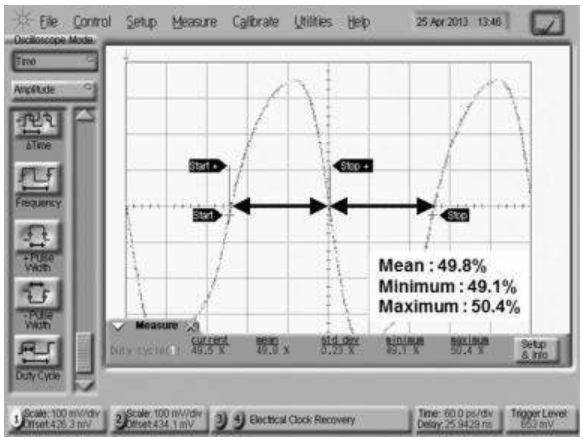
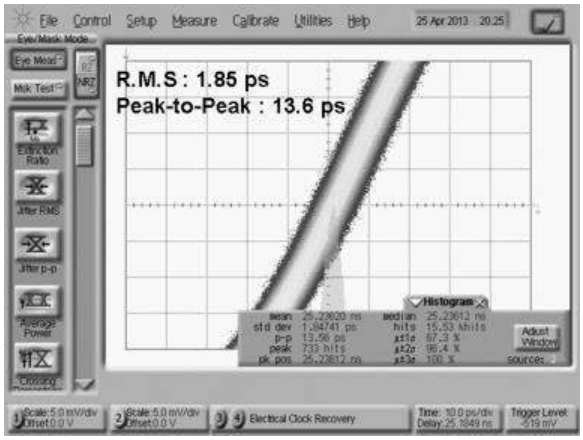
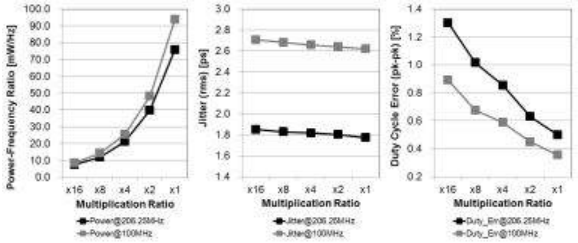
to low power SoC design than the multiplying DLL and the PLL, because the DLL core can be shared with other essential building block in SoC such as a temperaturesensor.









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VI. CONCLUSION

In this paper, a frequency multiplier for a DLL-based clock generator is proposed. The proposed HSHC-EC guarantees high-speed operation owing to its hierarchical edge-combiner structure and highly reliable operation owing to its use of an overlap canceller. The optimized pulse generator and the multiplication- ratio control logic are proposed to reduce the delay difference between positive- and negative-edge generation paths. Finally, a numerical analysis is performed to validate its performance. The frequency multiplier, which is fabricated using the 0.13-μm CMOS process technology, has the multiplication ratios of 1, 2, 4, 8, and 16, an output range of 100 MHz–3.3 GHz, and a power consumption to frequency ratio of 2.9 μ W/MH.

REFERENCES

[1] C. Kim, I. C. Hwang, and S.-M. Kang, "A low-power small-area + or - 7.28-ps-jitter 1-GHz DLL-based clock generator," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1414–1420, Nov. 2002.

[2] T.-C. Lee and K.-J. Hsiao, "The design and analysis of a DLL-based frequency synthesizer for UWB application," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1245–1252, Jun. 2006.

[3] C.-C. Wang, Y.-L.Tseng, H.-C. She, and R. Hu, "A 1.2 GHz Programmable DLL-based frequency multiplier for wireless applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 12, pp. 1377–1381, Dec. 2004.

[4] Christo Ananth, Bincy P Chacko, "Analysis and Design of Low Voltage Low Noise LVDS Receiver", IOSR Journal of Computer Engineering (IOSR-JCE), Volume 9, Issue 2, Ver. V (Mar - Apr. 2014), PP 10-18.

[5] Kyungh o Ryu, Jiwan Jung, Dong-Hoon Jung, Jin Hyuk Kim, and Seong-Ook Jung, *Senior Member, IEEE, frequency multiplier and DLL based clock generator.*

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Vol.3, Special Issue.24, March 2017

[6] B.H.Nagpara1 , Karan M. Jani2, D.N.Khandhar3 *Design and implementation of "DELAY LOCKED LOOP (DLL) using cmos sub nano meter technology.*
[7] K. Ryu, D. H. Jung, and S.-O. Jung, "A DLL with dual edge triggered phase detector for fast lock and low jitter clockgenerator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 9, pp. 1860–1870, Sep. 2012.
[8] I. Sutherland, R. F. Sproull, and D. Harris, *Logical Effort: Designing Fast CMOS Circuits*. San Mateo, CA, USA: Morgan Kaufmann, 1999.