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A 22nm INTEGRATED SUPPLY VOLTAGE TEMPERATURE VARIANT RELAXATION OSCILLATOR FOR BIOMEDICAL SYSTEMS

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ABSTRACT

A 22nm Integrated Supply Voltage Temperature Variant Relaxation Oscillator for biomedical systems has been presented. Concepts of dynamic threshold and switched resistors are proposed to improve the frequency stability against power supply and temperature variations, respectively. This design was verified in a 22nm standard CMOS process with 2 V supply. Measurement results show the frequency drift of 0.6% from 2V and temperature stability of 53.9 ppm/°C as temperature varied from −30 °C to 120 °C at a typical working frequency of 4 MHz. With the consideration of resistor and transistor matching, the oscillator was implemented in a core area of 0.05 mm2. The concepts of dynamic threshold (DT) and switched resistors (SRs) techniques are introduced to make the oscillator immune to voltage and temperature variations, respectively. These techniques minimize the frequency drift caused by supply variation as well as by temperature changes at the price of higher design complexity and larger chip area. The proposed SRs concept is aimed at making oscillation frequency insensitive to temperature in a process providing at least two types of resistors with different TCs.Index Terms Biomedical systems, clock generator, dynamic threshold (DT), frequency stability, relaxation oscillator, switched resistors (SRs).

INTRODUCTION

Nowadays, the increasing concern of people about health has boosted researches on devices and circuits for biomedical systems. As one of the most important modules in these systems, fully integrated high-stability oscillators are highly desired. Crystal oscillators have the best performance not only in phase noise and jitters, but also in stability against environment variations, such as process, supply voltage, and temperature (PVT). However, the external bulky devices lead to excessive costs and integration problems. In biomedical applications, such as the collection of life parameters and the check of functioning of living organism, more concern is focused on the stability of oscillators against PVT variations rather

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than jitters or phase noise , . Biomedical armamentaria with wide working temperature range are more attractive for better reliability in biological applications under harsh conditions. In addition, operating with wide range of supply voltage is also appreciated to extend the working time when powered by sources with finite energy. Given the above requirements, relaxation oscillators are more valuable as on-chip clock generators embedded in biomedical systems

SCOPE OF THE PROJECT

Many research activities have been carried out on high-stability relaxation oscillators. Some works concerned about performance in ultrahigh temperature environment for industrial applications. Some oscillators employed external components, external voltage references, and even sensors to achieve frequency stability against PVT. The most common way to realize a fully integrated high-stability oscillator is in the form of employing band gap voltage references (BGRs) or current reference. An alternative way of maintaining temperature stability is by utilizing mixing resistors, such as poly-to-poly or poly-to-diffusion, with opposite temperature coefficients .Recently, a relaxation oscillator that utilizes electron mobility as a time reference has been reported, which, as opposed to mixing resistors, is less suffered from process variations at the cost of degraded temperature stability. In this brief, a fully integrated high-stability relaxation oscillator suitable for biomedical systems under harsh conditions is presented. The concepts of dynamic threshold (DT) and switched resistors (SRs) techniques are introduced to make the oscillator immune to voltage and temperature variations, respectively. Experimental verification of the oscillator shows good agreement with simulation results. The oscillator exhibits a frequency drift of 0.6% from 2.4 to 4.0 V and temperature stability of 53.9 ppm/°C from −30 °C to 120 °C. This brief is organized as follows. Section II begins with a brief review of the conventional relaxation oscillator followed by the description of the concepts of DT and SR.

EXISTING SYSTEM

A fully integrated high-stability relaxation oscillator suitable for biomedical systems under harsh conditions is presented. The concepts of dynamic threshold (DT) and switched resistors (SRs) techniques are introduced to make the oscillator immune to voltage and temperature variations, respectively. Experimental verification of the oscillator shows good agreement with simulation results. The oscillator exhibits a frequency drift of 0.6% from 2.4 to 4.0 V and temperature stability of 53.9 ppm/°C from −30 °C to 120 °C. This brief is organized as follows. Section II begins with a brief review of the conventional relaxation oscillator followed by the description of the concepts of DT and SR. The measurement results and analyzes are assigned.

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DT TECHNIQUE

The circuit implementation of DT shown in the Fig. 3.1. The circuit consists of a timing capacitor, a timing resistor, some batches of current, and only one comparator. Oscillation is performed by periodically charging and discharging the capacitor as shown in the Fig. 3.1 follows.

1) At the beginning of power on, V_A, the voltage of node A in rises quickly to VOH = $V_{DD}-I_1 \cdot R$ while V_B, the voltage of node B, grows slowly with IC due to the large capacitor load. During this interval, the comparator output keeps switches OFF.

2) When $V_B > V_A = V_{OH}$, the comparator output flips over and turns the switches SC and SG on. Then, VA drops rapidly to $V_{OL} = V_{DD} - (I1 + I2) \cdot R$. In this duration, the charges in capacitor are drained out resulting in a decrease of VB. The state of oscillator changes to the discharging phase.

3) When $V_B < V_A = V_{OL}$, the comparator output turns the switches off again. Thus, the state of the oscillator returns to the charging phase. By inspecting the above operating mechanism, both high and low threshold voltages are dynamic and temporal. Although both V_{OH} and V_{OL} are related to supply voltage, the difference between them, $V_{OH} - V_{OL} = I_2 \cdot R$, is independent of the power supply with a simple self-biasing current source shown in Fig. 3.1.

According to the DT technique, the oscillation period can be R, C, I_C , $I_{1,2}$, and tp are the timing resistance, timing capacitance, charging current, currents for DT generation, and delays of comparator, respectively. In applications of several MHz, tp is negligible with sufficient gains of the comparator, which is primary contributor to power consumption and would consume hundreds of μA currents at frequency bands of MHz. In this design, tp is 1.74 ns with temperature drift of 12.81% from −40 °C to 120 °C. In addition, implies that DT actually allows all currents in the circuit with arbitrary characteristics as long as all of them are replicas of the same current source, which is I_S.

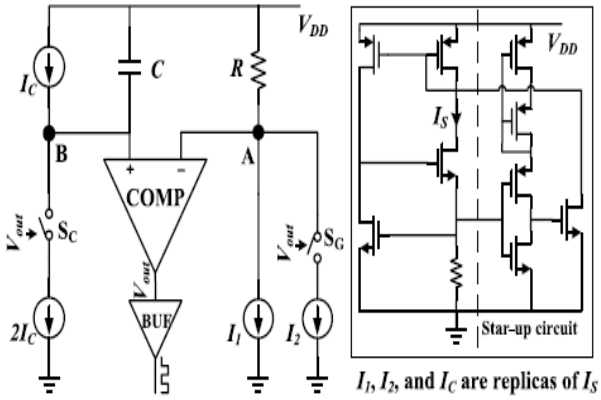

Figure 1 Schematic illustration of the proposed DT technique and bias circuits.

PROPOSED SYSTEM

The SR is proposed to mitigate the frequency drift of the oscillator when temperature changes. Temperature dependence of frequency is mainly caused

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by the large TC of resistors applied in the circuit. Mixing resistors with opposite TCs are commonly adopted to suppress the effect. However, almost all standard CMOS processes offer more than one type of resistors without ensuring the positive and negative TCs to be concurrent. The proposed SRs concept is aimed at making oscillation frequency insensitive to temperature in a process providing at least two types of resistors with different TCs.

SR TECHNIQUE

The proposed SR technique shown in the Fig. 4.1, Resistor R has been replaced by R_1 and R_2 with different TCs. In addition, a switch, S_R, is added in parallel to R_2. Control signals are derived from the output of comparator. The selection of Vout+/Vout− is determined by the polarity of TCs of R_1 and R_2.

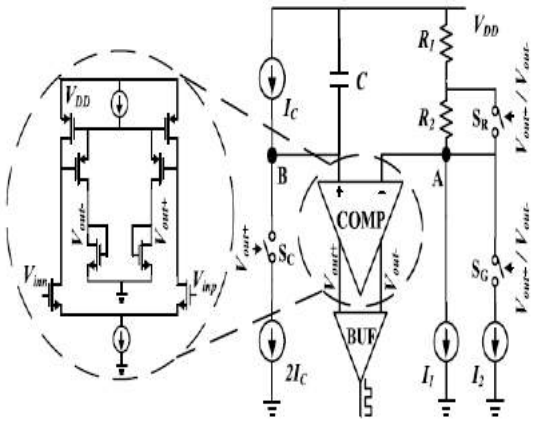

Figure 2 Circuit schematics of the proposed SR technique

MODES OF OPERATION

TCs of R_1 and R_2 Have the Same Polarity: In this case, the steering signals of switches, S_R and S_G, must be the same.

TCs of R_1 and R_2 are in Opposite Polarities: In this case, the high and low threshold voltages are, respectively, delivered as $V_{OH} = V_{DD} - I_1 \cdot R_1$ and $V_{OL} = V_{DD} - (I_1 + I_2) \cdot (R_1 + R_2)$ with Vout− being the command of SR.

TCs OF R_1 AND R_2 HAVE THE SAME POLARITY

In this case, the steering signals of switches, S_R and S_G, must be the same. The high threshold voltage and low threshold voltage are given by $VOH = VDD - I_1 \cdot (R_1 + R_2)$ and $V_{OL} = V_{DD} - R_1 \cdot (I_1 + I_2)$, respectively, with assumption of $R_1 \cdot (I_1 + I_2) > I_1 \cdot (R_1 + R_2)$. Besides, Vout+ must be taken as the dominator of S_R and S_G for correct charging/discharging timing. If $R_1 \cdot (I_1 + I_2) < I_1 \cdot (R_1 + R_2)$, not only should expressions of V_{OH} and V_{OL} be interchanged with each other, but also the determiners of S_R and S_G need to be changed to Vout−. Given the aforementioned conditions and with tp being ignored, the expression of oscillation period in should be modified correspondingly as shown in the Fig. 4.1

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As TCs of capacitor and the second-order TCs of resistors are ignorable with respect to the first-order TCs of resistors, the oscillation period in terms of temperature can approximately be with $R_x = R_{x0} \cdot (1 + TC_1|R_x \cdot \_T)$ and $\_T = T - T_0$, in which R_{x0}, $TC_1|R_x$, and T_0 are inherent resistance, the first-order TCs of resistors, and room temperature, respectively.

By defining the ratios of currents, resistors, and TCs as $I_C = \alpha \cdot I_S$, $I_1 = \beta \cdot I_S$, $I2 = \gamma \cdot I_S$, $R_{20} = m \cdot R_{10}$, and $TC_1|R_2 = n \cdot TC_1|R_1$ ($n \_= 1$).

TCs OF R1 AND R2 HAVE THE OPPOSITE POLARITY

In this case, the high and low threshold voltages are, respectively, delivered as $V_{OH} = V_{DD} - I_1 \cdot R_1$ and $V_{OL} = V_{DD} -(I_1 + I_2) \cdot (R_1 + R_2)$ with Vout− being the command of SR. To ensure proper charging/ discharging timing, SG must be controlled by Vout+. By the same defining terms of currents, resistors, and TCs, the oscillation period with respect to temperature. Except that n is negative for the opposite TCs of R_1 and R_2, other items have the same meaning as those in Case 1 as shown in the Fig. 4.2 . Simulation results show that the frequency characteristics of Case 1 and of Case 2 with supply voltage variation are close to each other. The VCs of the two cases are 0.82% and 0.84%, respectively, for voltage ranging from 2.0 to 4.0 V. The frequency drift of Case 1 is 75.6 ppm/°C which is larger than 52.7 ppm/°C in Case 2 for temperature varying from −40 °C to 120 °C.

SIMULATION IMPLEMENTATION

The SR is proposed shown in the Fig. 7.1 to mitigate the frequency drift of the oscillator when temperature changes. Temperature dependence of frequency is mainly caused by the large TC of resistors applied in the circuit. Mixing resistors with opposite TCs are commonly adopted to suppress the effect. However, almost all standard CMOS processes offer more than one type of resistors without ensuring the positive and negative TCs to be concurrent. The proposed SRs concept is aimed at making oscillation frequency insensitive to temperature in a process providing at least two types of resistors with different TCs.

The circuit schematic of the proposed SR technique. Resistor *R* has been replaced by *R*1 and *R*2 with different TCs. The selection of *V*out+/*V*out− is determined by the polarity of TCs of *R*1 and *R*2. The performance of the oscillator has been validated using measurement result.

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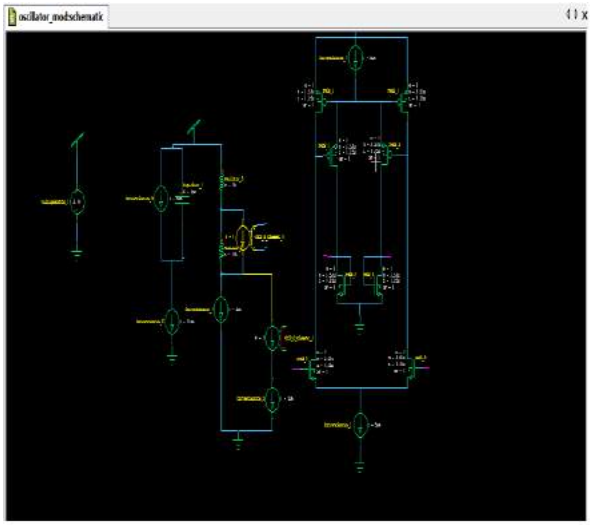

Figure 4 Schematic of the proposed SR technique.

T-SPICE:

The T-Spice simulation, specifies the number of components included and simulate the circuit schematics as shown in the Fig. 7.2.

List of terminals, and three subcircuit parameters. The terminals do not have a predefined order, but whatever order is used in the definition must be used in instances.

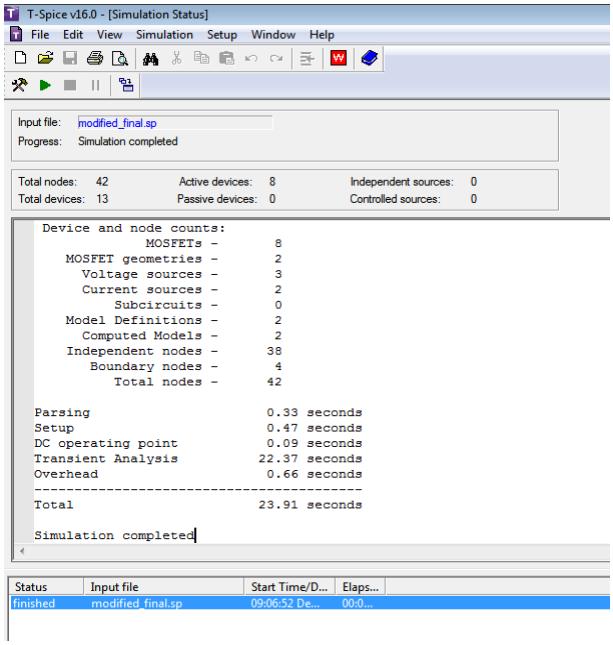

Figure 5 T-Spice Simulation of SR Circuit Schematics

CONCLUSION

A 22nm Integrated Supply Voltage Temperature Variant Relaxation Oscillator for biomedical systems is presented. Application of the DT technique simplifies the design of bias circuits and makes the BGR redundant with favourable frequency stability of 0.6% against power supply variation of 1.4 V. In addition, that the SR technique adopted in this design has no special requirements for resistors makes the oscillator be generally produced and applied in most of CMOS technologies. The oscillator is implemented in a standard 22nm CMOS process with a core area of 0.05mm2 .The measurement results indicate that the oscillator can operate under a wide temperature range with a frequency drift of 53.9 ppm/°C. Such a high-stability oscillator

can work in biomedical systems operating under harsh conditions.

Application of the DT technique simplifies the design of bias circuits with favorable frequency stability of 0.6% against power supply variation of 2 V. The SR technique adopted in this design has no special requirements for resistors makes the oscillator be generally produced and applied in most of CMOS technologies.A high-stability oscillator can work in biomedical systems operating under harsh conditions.

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Biography:

Parthiban K G received his ME in Process Control & Instrumentation from Annamalai University (2005) and persuing his PhD degree in Computer Science Engineering from Anna University, Chennai (Jan 2009). He is currently serving as Associate Professor in MPNMJ Engineering College,

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Chennimalai, Erode. He has 11years of teaching experience. He has published more than 25 research papers in various National and International conference proceedings. Also he published One books on "Electric Circuits and Electron Devices" from Sri Krishna publishers, Chennai. Also he published four national journals in Bio Medical field. His area of interest includes Soft Computing techniques and Bio medical signal processing.

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