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POWER DELAY PRODUCT AND AREA REDUCTION OF FULL ADDERS USING SYSTEMATIC CELL DESIGN METHODOLOGY

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Abstract— **In the modern electronic industry, low power circuit design has emerged as a most important topic for high speed and portable applications. Improvement of energy efficiency is one of the most serious features of modern electronic system designs. Minimization of circuit area and power consumption makes a device as a compact, reliable and efficient. The least amount of power utilization was a major driving force following the advance of CMOS technologies. The main objective of this project to investigate and compare the performance of XOR /XNOR based full adder using Systematic Cell Design Methodology. We implement and optimize the proposed 8 bit adder design circuit using Micro wind software tool. Here we will concentrate to improve the Area minimization and low power consumption based on SCDM (Systematic Cell Design Methodology.**

Keywords— **SCDM, Area minimization, Microwind, CMOS, XOR/XNOR**

I. INTRODUCTION

Power consumption and Delay are two important considerations for VLSI system design Engineers. Our prime motive is to reduce the power and to get less delay that is nothing but high speed for any design. Adder is one of fundamental block of Arithmetic Logic unit(ALU). In present arena we need fast arithmetic computation cells like adder and multipliers in the very large scale integration (VLSI) designs. The XOR-XNOR circuits are basic building blocks in various circuit especially-Arithmetic circuits (Full adder, and multipliers).To perform an arithmetic operation, mainly even a small circuit can consume very low power at extremely low frequency and also it may even take a long time to complete that operation. There are some standard implementations. Some different logic styles have been used in the past times for design of the full-adder cells. Although they are used for producing similar function and the way of producing transistor count and intermediate nodes are varied. Different logic styles have different advantages such as the size, power dissipation, speed and the wiring complexity of the circuit. The performance of the complex logic circuits is affected by the individual performance of the XOR-XNOR circuits Therefore, careful design and analysis is required for XOR-XNOR circuits to obtained –full output voltage swing, lesser power consumption and delay in the critical path. Additionally, the design should have a lesser number of transistors to implement XOR-XNOR circuits.

II. PREVIOUS FULL-ADDER OPTIMIZATIONS

CMOS logic styles have been used to implement the low power 1-bit adder cells. In general, they can be broadly divided into two major categories: the Complementary CMOS and the Pass-Transistor logic circuits. The complementary CMOS (C-CMOS) full adder (Figure 1) is based on the regular CMOS structure. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor sizes.

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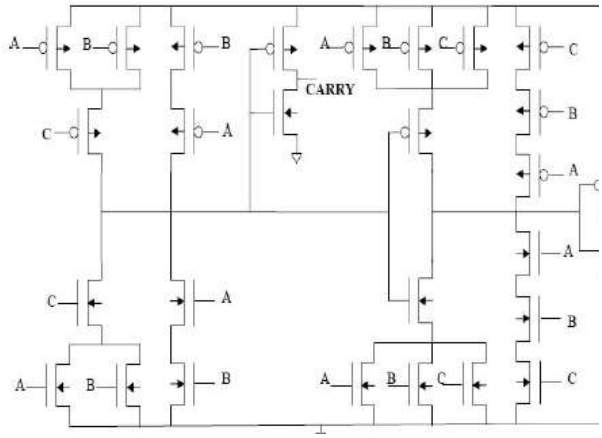

Fig.1 C-CMOS Full Adder Cell.

The equation for C-CMOS is given as below

Sum = ABC + AB'C' + A'BC' + A'B'C &
Sum =Carry'.(A+B+C) + (A.B.C)

From the equation we have drawn the pull up and pull down networks and from that we have generated the sum and carry outputs. The advantages of the complementary CMOS logic circuit are stability and layout regularity at lower voltages due to smaller number of interconnecting wires and complementary pairs of transistors. The C_CMOS have some robustness against transistor sizing and voltage scaling which can have reliable operation at very low voltages with different transistor sizes.

III.XOR/XNOR CIRCUIT DESIGN

Exclusive–OR (XOR) and Exclusive-NOR (XNOR) circuits implement functions that are complementary. XOR and XNOR, denoted by ⊕□ and ⊙ respectively, are binary operations that perform the following Boolean Functions

$$x \oplus y = x'y + x\,y'$$
$$x \odot y = x\,y + x'y'$$

In the past two decades, a number of circuit techniques have been reported with a view to improve the circuit performance of XOR-XNOR gates.

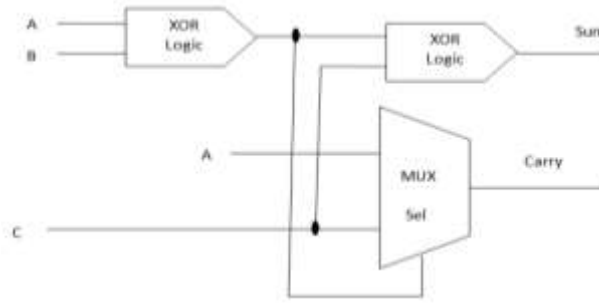

Fig.2 Three-input XOR circuit.

A wide variety of XOR-XNOR implementations are available to serve different speed and density requirements. Instead of cascading two 2-input XOR gates, a new design for 3-input XOR/XNOR circuit is given. The reported circuit has the least number of transistors and no complementary input signals are needed. Especially, the power-delay product is also minimized

IV.SYSTEMATIC CELL DESIGN METHODOLOGY

SCDM (Systematic Cell Design Methodology), which is an extension of CDM, plays the essential role in designing efficient circuits. As an especial feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay, low VDD operations, low static power dissipation, avoids any degradation on the output voltage, increased the driving capability. After the systematic generation, the SCDM considers circuit optimization based on our target in three steps:

1) wise selection of the basic cell
2) wise selection of the amend mechanisms
3) Transistor sizing.

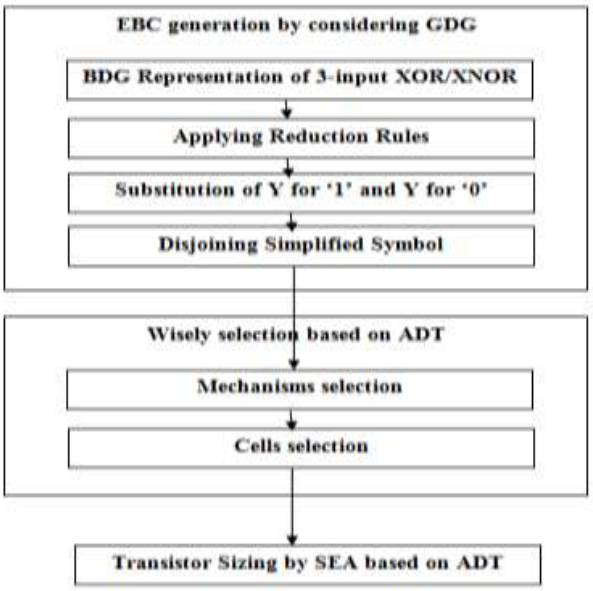

Fig.3 (a) Flowchart for EBC

A.EBC GENERATION

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In order to generate the EBC(Elementary Basic cell) of Three -input XOR/XNOR circuits ,four steps are taken. Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. Afterward, as the inputs into the first level are 0's and 1's of the function's truth table, the 0 and 1 can be replaced by the *Y* and *Y′*, respectively. In the process of designing balanced 3- input XOR–XNOR circuits, we face three independent inputs and two complementary outputs. The result of applying the reduction rules and the substitution and disjoining to the trees. Hence the tree becomes, The elementary basic cell which is extracted of minimum sum of product form of 3-input XOR– XNOR has been presented. This cell has eight elements, deciding two outputs. Each element is a pass transistor or transition gate and has two input controls, i.e., the gate and either the drain or the source. The input signals (applied to the two input terminals of these transistors) and the selection of PMOS, NMOS transistors This cell has eight elements, deciding two outputs.[8]We refer to the pins of the central section (IN1–IN4 and G1–G4) as *A* or *C*, or their complements. We also assume that pins of the external section *G*5–*G*8 can also be *B* or its complement. This form of the circuit (as the elementary basic cell) is power-less and ground-less(P-/G-).

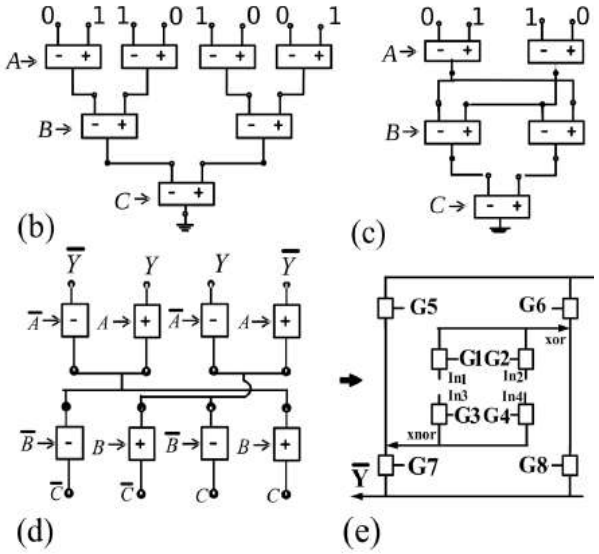

Fig.3(b): BDT representation of three-input XOR /XNOR function. (c) Applying reduction rules. (d) Substitution and disjointing. (e) EBC.

B. WISELY SELECTION OF MECHANISMS AND CELLS BASED ON DESIGN TARGET

By replacing the elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is meditated to determine dominant mechanisms and cells, in terms of power, and delay when the optimization goal is PDP. The results are used to produce circuits for high-performance portable electronic applications. Mechanisms include optimization mechanisms to resolve non full swing ,correction mechanisms to resolve high impedance. The cells are divided into two categories:

- ✓ cells with both nMOS and pMOS in EBC structure
- ✓ only nMOS

To reduce complexity, we have also considered the central part of EBC and to achieve real results. Using transmission gates in EBC, which is called TG, the complete circuit is achieved as there is no need for any other mechanisms. Hence the New 3- input XOR/XNOR circuits are implemented which is shown in the below fig.4. This should be drawn on the basics of systematic cell design methodology using elementary basic cell.

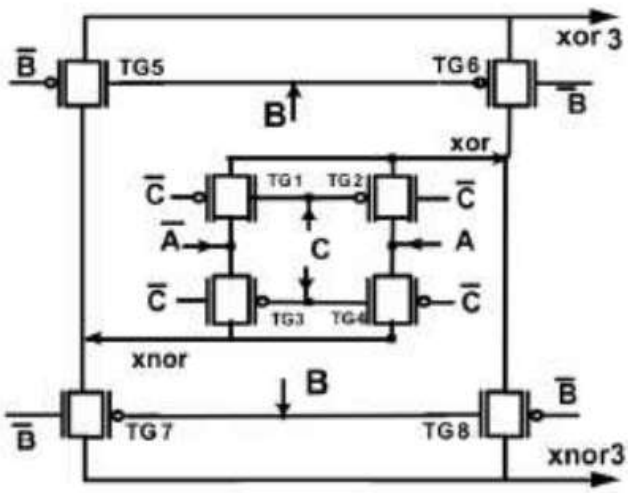

Fig.4: New 3 input XOR/XNOR based 1 bit adder

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V.PROPOSED FULL ADDER DESIGN

A 4 bit ripple carry adder is implemented as an extension to the proposed 1 bit full adder. The carry propagates all the way to the last adder in the ripple carry adder structure. The performance evaluation is carried out using 45 nm technology. The 4 bit structure of the proposed adder is compared with CMOS adder. It is observed that the four bit structure of proposed adder is efficient compared to the CMOS adder with respect to average power, average carry propagation delay and PDP.

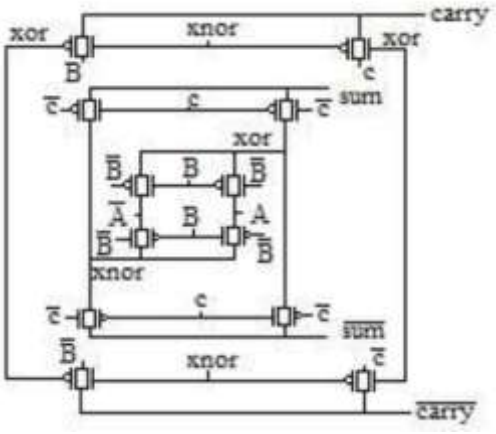

Fig.5: Four- bit ripple carry adder

VI. SIMULATION RESULT

Reduction of power consumption provides a great improvement to an adder circuit. Power consumption issues can lead to over consumption of resources when devices are cascaded. This reduction in power would come at the expense of overall speed and increased delay. On the basis of Microwind designing tool we make the performance comparison between of area and power of CMOS full adder by proposed 3-input XOR/XNOR full adder design which consist 16 transistors. In order to compare the results of the proposed full adder circuits with the existing full adders, a wide range of experiments was carried out. Schematics are designed for all the circuits using Microwind for 45nm technology.

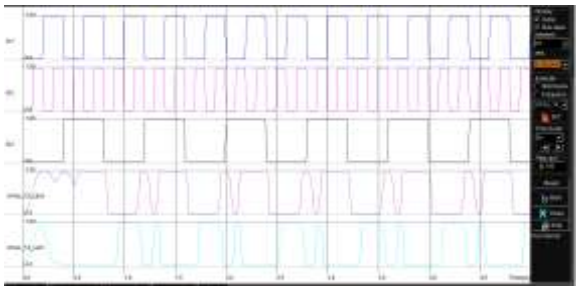

Fig.6: input and output waveform results for C-CMOS full adder

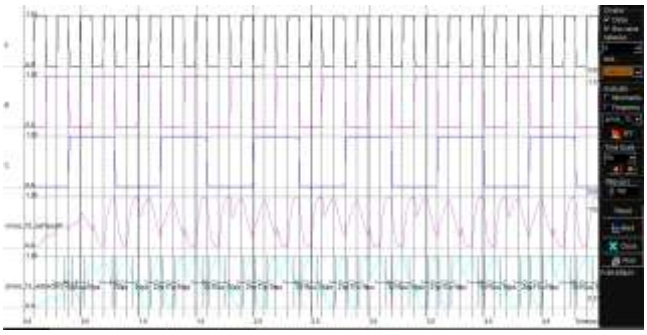

Fig.7 input and output waveform results for 3-input XOR/XNOR based full adder

TABLE I

Type of Adder	Power(mW)	Delay(ps)	PDP
C-CMOS Adder	0.104	50.899	0.529
Proposed 1 bit Adder	0.098	48.820	0.478
Proposed 4 bit adder	0.14578	53.820	0.078

It has been shown that proposed adder circuit show less power consumption and delay than previously reported adders. Proposed full adder has less internal capacitance as number of transistors is reduced and gives reduced power consumption.

VII.CONCLUSION

In this paper a 1 bit full adder is proposed using SCDM which is later extended to 4 bit ripple carry adder. The simulation was done using Micro wind tool with 45 nm technology and compared with existing C-

CMOS adders The use of SCDM as the design methodology ensures a symmetric and power-ground free structure & exhibiting 27%–77% reduction in average energy-delay product. The simulation results prove that the proposed adder offer improved PDP compared to existing CMOS adder.

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