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A LOW POWER NON-VOLATILE LOGIC GATE USING SWAPPED CMOS TECHNOLOGY

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ABSTRACT

Field programmable gate array (FPGA) can be customized to user applications and provide improvement in power efficiency over CPUs and high overhead for flexibility. The NVMs also have the desirable property of non volatility, which means that they can be turned off during standby to save power. Here we introduce a low power non-volatile logic gate using swapped CMOS technology. To design the non volatile memory of RRAM based on swapped MOS technology and to reduce power consumption. Non volatile memories are STT-MRAM AND OxRRAM. Here already used programmable interconnects process. Because programmable interconnects majestic part of FPGA. An interesting application of resistive switching is the fabrication of novel non volatile resistive random access memories.

Keywords: - FPGA, NVM (Non Volatile Memory), RRAM, MOS Technology.

I.INTRODUCTION

Field Programmable Gate Arrays are main part of the digital circuits or systems. FPGA architecture has a drawbacks on the quality of the final products speed performance, power consumption and area efficiency. Mainly using emerging nonvolatile memory (NVM) technology. Because it gives new opportunities for design improvement. In this paper based on RRAM based programmable interconnects which is permit by using the RRAM properties. RRAM based interconnects are constructed by three separate structure. transistors Programmable interconnects, a programming and on demand buffering architecture. Transistor programmable interconnects are constructed by RRAMs and metal wires only and are placed on atop of CMOS transistors. The RRAMs are shared via transistor programmable interconnects by using programming grid. On demand buffering architecture an gives opportunity to dispense buffers in interconnect during implementation phase.

The conventional FPGA has three basic blocks. In this three blocks are Connection Block(CB), Logic Block(LB) (also called Configurable Logic Block) and Switch Block. In this LB contains Basic Logic Elements like Look Up Table (LUT), MUX and Buffer. Logic functions are taken from the Look up Tables. And LB block include local routing multiplexers (MUXs). It provided connection between BLEs.

In this three component having some limitations.That limitations are 1. most of the FPGAs are used SRAM. It store programming bits and include six transistor in single SRAM. But modern FPGA having bitstream programming so it having excessive power consumption. 2. Large foot print.

In (1) based on the novel spin transfer torque (STT) writing approach, which has been recently introduced and developed , reduces significantly the switching energy and data disturbance when compared with the conventional MTJ writing approach. It reduces power consumption but complexity is high.

In (2) this paper reports a 45nm spin transfer torque(STT) MRAM embedded into a standard CMOS logic platform that employees low power (LP) transistors and Cu/low-k BEOL. The first ever demonstration of embedded STTMRAM that is

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fully compatible with 45nm logic technology. The system speed to be high and it consumes more area.

ARCHITECTURE DESIGN

First we decide which kind of NVM to use in this process. Different kind of NVMs are STTRAM, PRAM and RRAM. STTRAM has an on/off ratio is below 10. But RRAMs have a very high on/off ratio(10^6).So it is used for routing switches. Programmable interconnect process based on transistor less programmable interconnects,

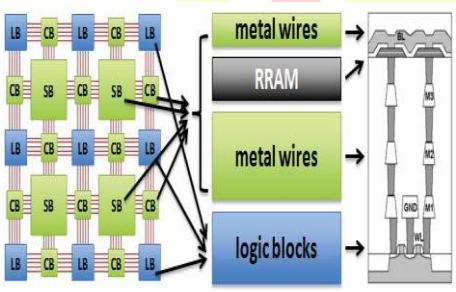

Fig 1:Architecture design

process. RRAMs are used to friendly layout design RRAMs and metal wires are placed on the CMOS transistor.

EXISTING METHOD:

The non volatile memories are used in this paper. The design based on CMOS technology. They are designed an RRAM friendly layout. In this design based on programmable interconnects process. Resistors are used to programmable interconnects.

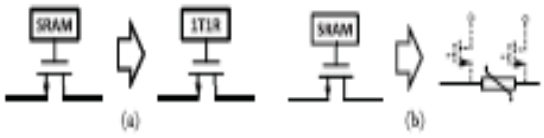

fig: 2 (a)Replace SRAM with NVMs (b) Use NVMs as programmable switches

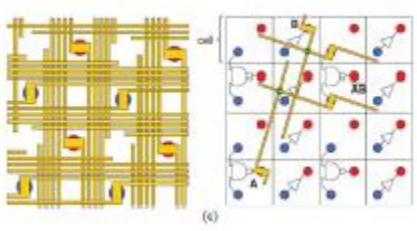

Fig 3: Field programmable nano wire interconnect

This existing system consumes more dynamic power dedicated to data transfer. So access low speed accelerate in synchronous NV logic gates based on RS memories. It require more area and power consumption level to be high is writing circuits for RS-NVM. So it will affect system performance, power, speed and system accuracy to be low. Here used advanced P&R tool named VPR_RPI. Because that was developed for novel structures. In this paper mostly analysis the theoretical analysis.

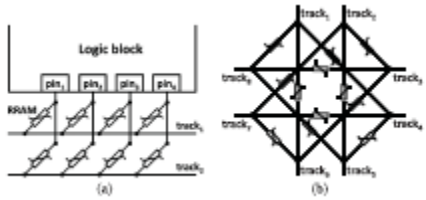

Fig 4: Programmable interconnect blocks

(a)RRAM based connection block. (b) RRAM based switch block

PROPOSED METHOD

Our proposed work is swapped MOS design for modified memory stage. This modifies design to optimize the CMOS NVM circuit. This implemented in memory unit and write logic by using tanner tool.

Write logic design is performed by using logic gates. Applying write signal through this write circuit. Then written bits in written circuit passed to RRAM circuit. When the written signal is 1 input data will read at the read port. Here we introduce Swapped MOS technology. Swapped MOS performs

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through the designed PMOS and NMOS combination.

In this, two terminal exchanging their flow of source, hence the required power will be reduced to circuit. Increase the power performance we modifies the memory and write circuit.

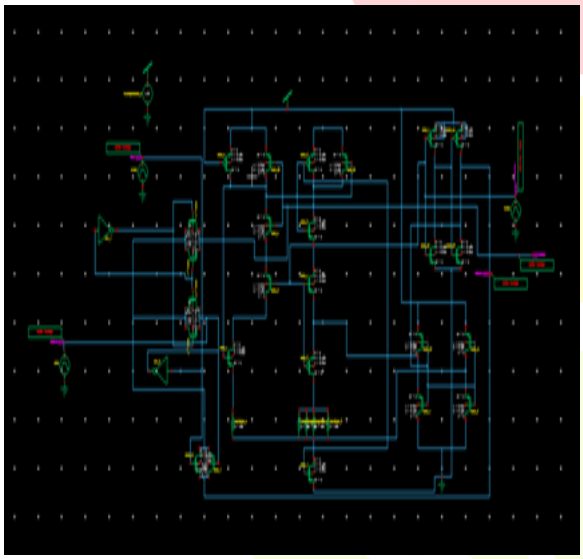
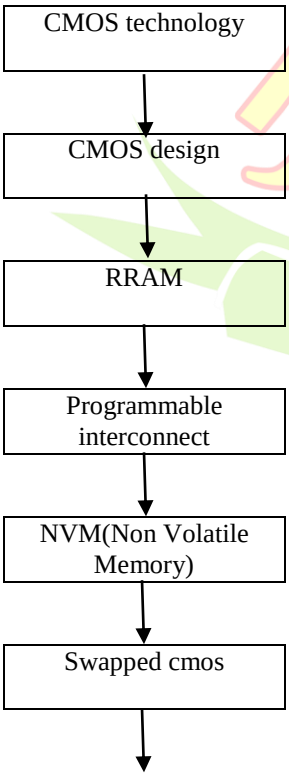


Fig 5:proposed method circuit diagram



Reduced power consumption and area

Fig 6: System flow design

The proposed method is a promising technology, which has complexity compared to existing system and high accuracy will be obtained. Swapped CMOS technology means exchange the PMOS and NMOS place depending upon the flow of source. It means two PMOS transistor combined to form a single CMOS transistor.so area will be reduced and power consumption also reduced.

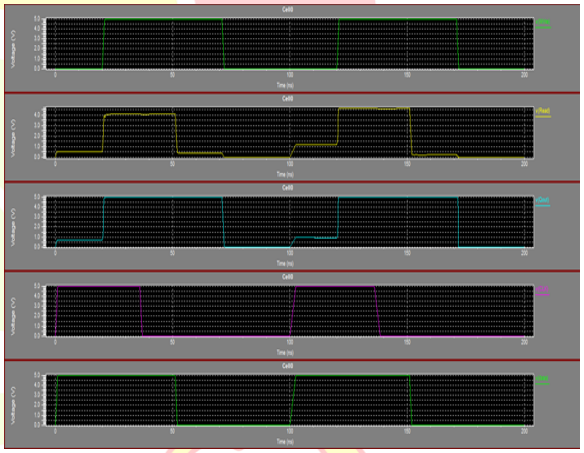


Fig 7: Result obtained from proposed circuit.

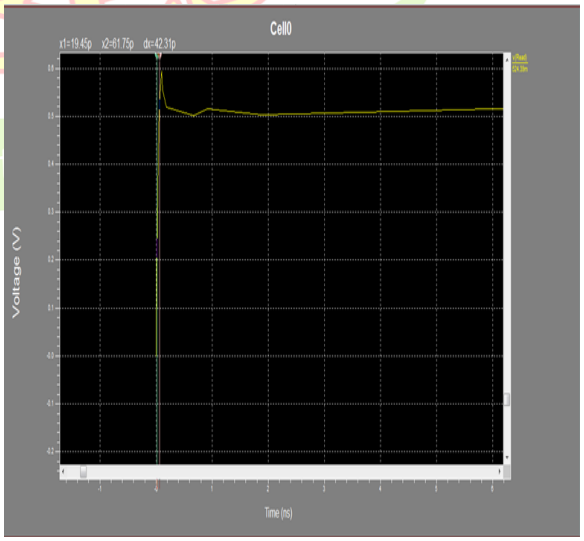


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Fig 8: Result of delay measurement.

RESULTS

Here reduced delay time and area efficiency from this paper. Existing method contain 102.9 ps in delay time but our proposed result is 43.4 ps. Area efficiency of existing method is 32nmx40nm our proposed method result is 29nmx40nm.

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