

# AN OPTIMIZED DESIGN OF CMOS ANALOG MULTI-FUNCTION CIRCUIT IN CURRENT MODE

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**Abstract**— This paper describes a CMOS analog circuit intended for multi-functions by utilizing the translinear principle of the MOS transistor operating in the subthreshold region. The circuit is designed and simulated using TSPICE simulator in 180nm standard CMOS technology. The simulation results of this circuit demonstrate a linearity error of 0.72%, a THD of 0.13%, a  $-3\text{dB}$  bandwidth of 1.5MHz and a maximum power consumption of  $1.08\mu\text{W}$ . This circuit is expected to be useful in analog signal processing applications.

**Keywords**— Amplifiers, Analog circuits, Current-mode Circuits, Multiplying circuits, Subthreshold, Translinear loop.

## I. INTRODUCTION

The evolution of integrated circuit technology and future scenarios of ubiquitous and pervasive computing have stressed the need of very low power and low voltage circuits with high signal dynamic range and linearity. An optimized current-mode analog computational circuits got an increasing interest especially as CMOS fabrication technology advances. Using current mode circuits, many functions can be designed with less number of components compared to its voltage-mode counterpart. Analog computational circuit is an essential building block of analog signal processing system. It has wide range of applications, particularly, in the fields of control, instrumentation, measurement and telecommunications.

The demand for portable operation of electronic systems has lead to the trend of designing circuits to be featured with low power dissipation and operate for low supply voltages. Many four-quadrant multipliers suitable for low-power dissipation and/or low-voltage operation have been developed

[9-11]. Among those reported works, the CMOS circuits operating in subthreshold region makes it is possible to realize low voltage and low power circuits. In [1] an OTA-based multiplier/divider is proposed. This method consumes more power than transistor level design. Another approach reported in [2] uses switched current technique. This approach suffers from noise associated with switching. In references [3-6], MOSFETs in saturation region are used to design some computational circuit. In [7], a floating-gate MOS transistors are used to implement a four quadrant multiplier. Implementing circuits using MOSFETs in saturation region consume more power. Several circuits were proposed in the literature that use MOSFETs in subthreshold. In [8] an approximation for logarithmic and exponential circuit is used to implement fractional power function. The multiplier circuit reported in [12], shows good linearity but the power consumption is high. Different methods for reducing power consumption have been proposed. They use FGMOS [13] bulk driven MOS, and class-AB mode. They suffer from speed constraints. The translinear principle using MOSFETs operating in subthreshold region is a promising technique reported in [14]. Once the translinear loop is formed both multiplication and division processes occurs essentially.

In this paper, An optimized design of current-mode circuit that can do five functions using CMOS transistors working in subthreshold region is proposed. The five functions are multiplier, divider, controllable-gain current amplifier, current-mode differential amplifier, and differential-input–single-output current amplifier. The rest of the paper is organized as follows. Section 2 describes the multi-function circuit. Simulation results are presented in Section. 3. Section 4 concludes the paper.

## II. CIRCUIT DESCRIPTION

The multifunction circuit proposed in this paper is shown below in Fig.1. It consists of two overlapping translinear loops formed by six-matched transistors. The transistors  $M_1$ ,  $M_2$ ,  $M_3$ , and  $M_4$  forms the first loop and transistors  $M_1$ ,  $M_3$ ,  $M_5$ , and  $M_6$  forms the second loop. All of these transistors are operating in subthreshold region makes it possible to achieve low power consumption.

By applying KVL to the two translinear loops yields the following

$$V_{SG1} + V_{SG2} = V_{SG3} + V_{SG4} \quad \text{Eq.1}$$

$$V_{SG1} + V_{SG5} = V_{SG3} + V_{SG6} \quad \text{Eq.2}$$

The drain current of a transistor biased in subthreshold region is given

$$\text{Eq.3}$$

where  $W$  and  $L$  are the channel width and length respectively,  $V_T$  is thermal voltage,  $n$  is the subthreshold slope factor, and  $V_{Th}$  is the threshold voltage [1] and  $I_{D0}$  is a process dependent parameter [5]. To keep the MOSFET working in subthreshold, then the drain current should be kept much less than the saturation current, ( $I_D = W/L \cdot I_{D0} \ll 1$ ). If  $V_{DS}$  is four times the thermal voltage  $V_T$  ( $V_{DS} > 100 - \text{mV}$ ), then, eq.3 can be reduced to

$$\text{Eq.4}$$

and the source-to-gate voltage is given by

$$\text{Eq.5}$$

Since all the transistors of the translinear loops are matched, and by substituting Eq.5 back into eq.1 and eq.2 yields equations 6 and 7

$$I_1 I_2 = I_3 I_4 \quad \text{Eq.6}$$

$$I_1 I_5 = I_3 I_6 \quad \text{Eq.7}$$

where,  $I_i$  is the drain current for the transistor  $M_i$ .

Let  $I_4$  be the output of the first translinear loop and  $I_6$  be the output of the second translinear loop. The difference between the two output currents is considered as the output of the proposed circuit. The output current is given by

$$I_{out} = I_4 - I_6 = I_1(I_2 - I_5)/I_3 \quad \text{Eq.8}$$

By modifying the input currents, the proposed circuit can implement many functions as will be shown in the next subsections.

#### A. Four-quadrant multiplier

By setting the currents  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_5$  to values shown below the multifunction circuit operates as four quadrant multiplier

$$I_1 = I_0 + i_{in1}$$

$$I_2 = I_0 + i_{in2}$$

$$I_3 = I_0$$

$$I_5 = I_0 - i_{in2}$$

The currents  $i_{in1}$ ,  $i_{in2}$  are AC input signals, and substituting the above values in eq.8, yields

$$I_4 - I_6 = 2i_{in2} + 2i_{in1}i_{in2}/I_0 \quad \text{Eq.9}$$

The output current becomes

$$I_{out} = 2i_{in1}i_{in2}/I_0 \quad \text{Eq.10}$$

It is very clear that this four-quadrant multiplier can implement squaring function if  $i_{in1} = i_{in2} = i_{in}$ , the output current is given by

$$I_{out} = 2i_{in}^2/I_0 \quad \text{Eq.11}$$

#### B. Two-quadrant divider

By setting the currents  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_5$  to values shown below the multifunction circuit operates as two quadrant divider

$$I_1 = I_{gain}$$

$$I_2 = I_0 + i_{in1}$$

$$I_3 = I_{in2}$$

$$I_5 = I_0 - i_{in1}$$

then the output is given by

$$I_{out} = 2I_{gain} \cdot I_{in1} / I_{in2} \quad \text{Eq.12}$$

It is clear that eq.12 implements a divide function with controllable gain.

#### C. Current mode differential amplifier

Similarly by setting the currents  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_5$  to following values, the proposed circuit can be used as Current mode differential amplifier

$$I_1 = I_{gain1}$$

$$I_2 = I_0 + i_{in1}$$

$$I_3 = I_{gain2}$$

$$I_5 = I_0 + i_{in2}$$

The currents  $I_1$ , and  $I_3$  are used to control the gain of the differential amplifier, the output current is given by:

$$I_{out} = I_4 - I_6 = I_{gain1} / I_{gain2} \cdot (I_{in1} - i_{in2}) \quad \text{Eq.13}$$

#### D. Differential input single output current amplifier

Similarly by setting the currents  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_5$  to following values, the proposed circuit can also be used as differential input single output current amplifier

$$I_1 = I_{gain1}$$

$$I_2 = I_0 + i_{in1}$$

$$I_3 = I_{gain2}$$

$$I_5 = I_0 - i_{in1}$$

The output current is

$$I_{out} = I_4 - I_6 = 2I_{gain1} / I_{gain2} \cdot (i_{in1} - i_{in2}) \quad \text{Eq.14}$$

#### E. Controllable gain current amplifier

By setting one of input currents to zero, a controllable gain amplifier is obtained and the currents are set to the following values:

$$I_1 = I_{\text{gain1}}$$

$$I_2 = I_0 + i_{\text{in1}}$$

$$I_3 = I_{\text{gain2}}$$

$$I_5 = I_0$$

The output current is

$$I_{\text{out}} = I_4 - I_6 = I_{\text{gain1}} / I_{\text{gain2}} \cdot (I_{\text{in1}}) \quad \text{Eq.15}$$

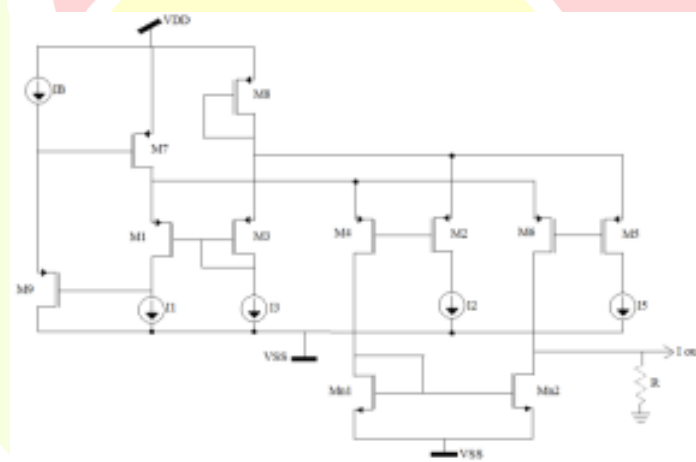


Fig 1 The analog multi function circuit

### III. SIMULATED RESULTS

In order to evaluate the proposed circuit, the CMOS analog multifunction circuit has been simulated with the tanner tpsice using 0.18μm CMOS technology.

The aspect ratios of the PMOS transistors  $M_1-M_6, M_a, M_b$  are  $(W/L) = (8/1)$  and transistor  $M_c$  is 0.3/1.8 and NMOS transistors are 0.5/9.

The circuit operates from ±0.6 V DC supply,  $I_B$  was set to 10 nA, and the input currents for the multiplier were swept from -20 to 20 nA. simulation result in fig.2 confirms the multiplication function and fig.3 confirms the squaring function.

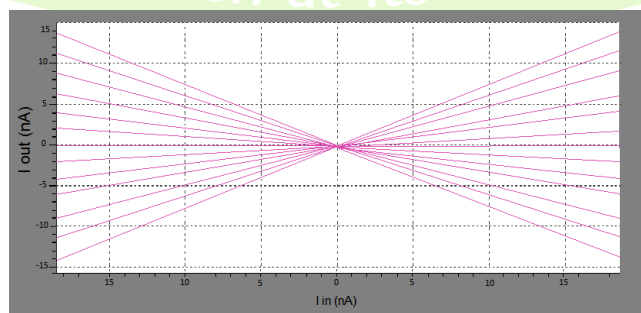


Fig 2 Multiplier DC transfer curve

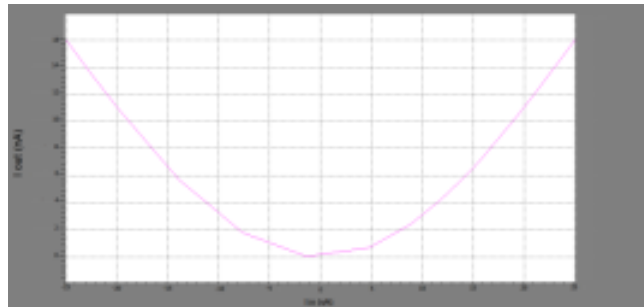


Fig 3 Squaring DC transfer curve

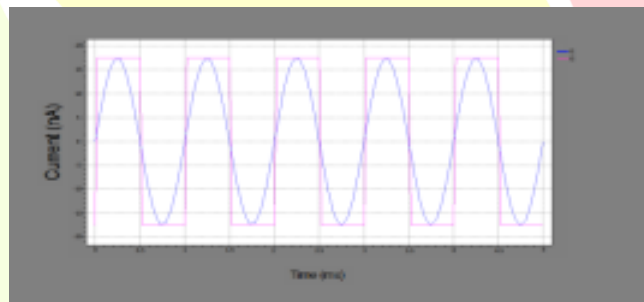


Fig 4(a) Simulation results of input signals in differential amplifier

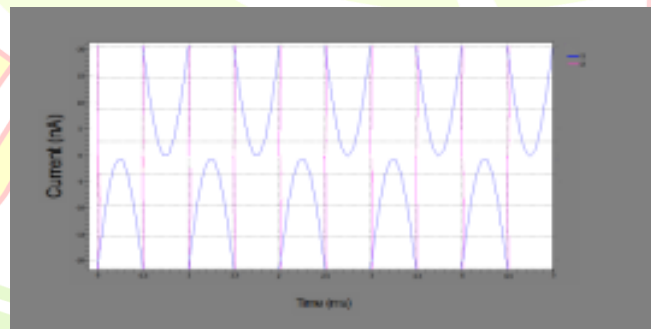


Fig 4(b) Simulation results of output signals in differential amplifier

Fig 4(a) and (b) shows the input and output current signals respectively in differential amplifier mode. This result confirms the differential amplifier operation by subtracting the square signal from the sinusoidal signal.

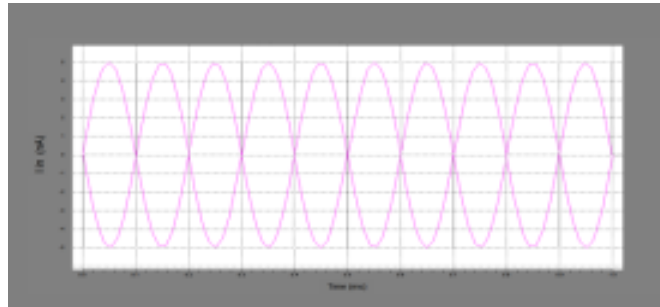


Fig 5(a) Simulation results for differential input single output amplifier input signals

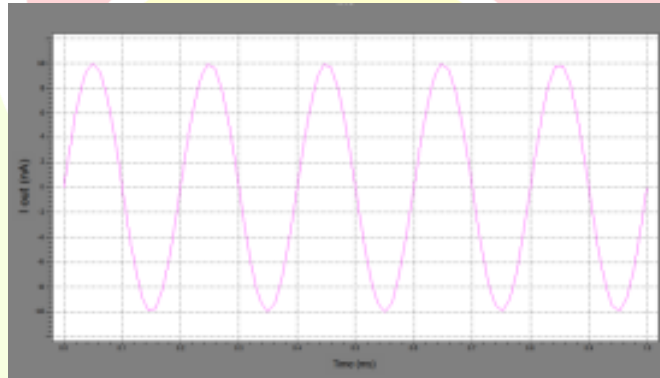


Fig 5(b) Simulation results for differential input single output amplifier output signals

Fig 5(a) and (b) shows the simulated results of differential input single output amplifier.

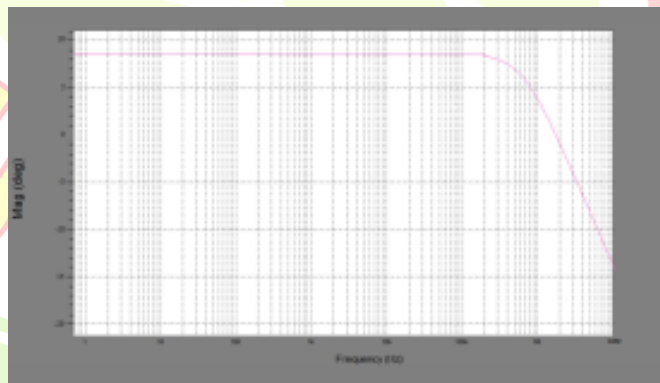


Fig 6 Frequency response of analog multifunction circuit.

When configured as an amplifier, the THD(total harmonic distortion) of the multifunction circuit is found to be 0.13% this was calculated by applying a sine wave with frequency of 1kHz and then calculating the ratio of power of the 1000 harmonics to the power of the fundamental frequency. The result shows that the -3dB frequency is around 1.5MHz and the calculated linearity error of 0.72%.

Table 1. Simulated parameters

Supply voltage(V)	0.6
Power consumption( $\mu$ W)	1.16
THD(%)	0.13

Bandwidth(MHz)	1.5
Linearity error(%)	0.72

#### IV. CONCLUSION

The CMOS analog multi-function circuit in current mode was presented using the translinear principle to reduce the supply voltage that leads to reduce the power consumption, which is essential today to increase the battery life time on most applications. This Circuit is capable of performing multiplication, division, controllable-gain current amplifier, current-mode differential amplifier, and differential-input–single-output current amplifier.

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