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DESIGN ANALYSIS OF SINGLE ENDED DYNAMIC FEEDBACK 12T SRAM CELL

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ABSTRACT:

This method presents a new bit-interleaving 12T sub threshold SRAM cell with Data-Aware Power-Cutoff (DAPC) Write-assist to improve the Write-ability to mitigate increased device variations at low supply voltage under deep processes. The disturb-free feature facilitates the bit-interleaving architecture that can reduce multiple-bit errors in a single word and enhance soft error immunity by employing error checking and correction (ECC) techniques. The proposed 12T SRAM cell is demonstrated by a macro implemented in CMOS technology. The test chip operates from typical (lower than the threshold voltage) with limited by Read operation. Data can be written successfully. The measured maximum operation frequency and total power consumption.

INTRODUCTION:

The usage of SRAM continuously increases in system-on-chip (SOC) designs. Recently, the demand for ultra-low power battery-operated devices is growing relentlessly, especially in implanted medical instruments and wireless body sensing networks where low supply voltage and low power SRAMs are required to extend system operation time under limited energy resources. Supply voltage scaling is the most effective way to reduce both switching power and leakage power for CMOS VLSI. However, designing robust SRAMs for near threshold or subthreshold operation is extremely challenging due to increased device variations and reduced design margins at low supply voltages with extremely scaled processes. The conventional 6T SRAM cell has a very simple structure. However, its operation margin suffers from Read disturb, Half Select disturb, and the conflicting Read/Write requirements. Moreover, due to increasing threshold voltage fluctuations caused by global and local process variations in advanced CMOS processes, the Read and Write stability of 6T SRAM degrade rapidly with scaling. Various Read/Write-assist schemes have been proposed for robust low-voltage operation.

These techniques include utilizing dual supply voltages to adjust the cell supply voltage, raising the cell virtual-VSS, reduced. However, the minimum operation voltage of the conventional 6T cell is limited to around. Read disturb is one of the constraint for of the conventional 6T cell. A 7T cell was proposed to mitigate Read disturb at the expense of Write-ability due to single-ended Write operation 8T and 10T cells with single-ended Read were also proposed. In these schemes, cell storage nodes were decoupled from the bit-line during Read operation to eliminate Read disturb and improve Read Static Noise Margin (RSNM). Furthermore, when SRAMs operate under near-threshold or subthreshold region, alpha-particles or energetic cosmic rays can potentially induce soft errors more easily because the critical charge is reduced. In this work, we propose a novel 12T bit-cell with a differential cross-point data-aware power-cutoff (DAPC) Write assist for low-voltage operation. During the Write operation, depending on data-in, the proposed bit-cell internally cuts off supply voltage for either the left or right half-cell to weaken the pull-up network of the bit-cell, thus assisting the discharging of the storage node. This proposed scheme improves Write-ability without employing additional peripheral Write-assist circuits and related boosting and timing control circuits. Furthermore, this bit-cell employs a cross-point Write structure with a data aware column-based Write Word-Line (WL) to eliminate Write Half-Select (WHS) disturb. Thus, the bit-cell supports a bit-interleaving architecture to improve soft error immunity.

EXISTING METHOD:

In the Existing method we used the system of SRAM cell designing in 6T and 8T.

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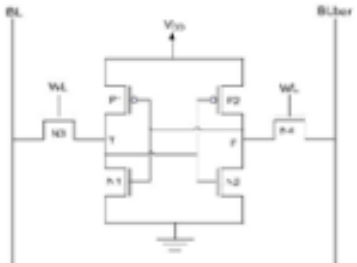

Fig.no 1: 6T SRAM cell

DISADVANTAGES:

- Estimation also showed a small error sigma<3%.
- The quantization noise imposed on such tiny current variation. Can quickly degrade the estimation accuracy.
- High power consumption
- Noise performance is not reduced
- Area is not reduced
- Accuracy is low

PROPOSED METHOD:

- In the proposed method we used the system of new bit-interleaving 12T sub threshold SRAM cell with Data-Aware Power-Cutoff (DAPC) Write-assist to improve the Write-ability to mitigate increased device variations at low supply voltage under deep processes.

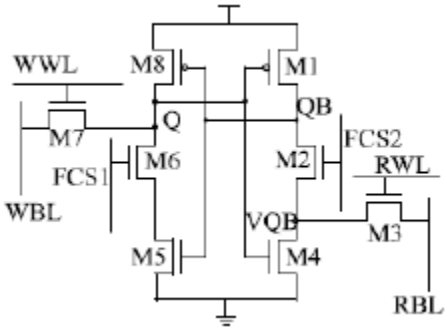

Fig.no 2: 8T SRAM cell

ADVANTAGES:

- Low power consumption
- Noise performance is reduced
- Accuracy is high
- Operating speed is high
- Leakage current is reduced

THE PROPOSED 12T SRAM CELL:

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The schematic and cell layout of the proposed 12T SRAM cell. The 12T SRAM cell consists of a core, PUL, SWL, PDL, PUR, SWR, and PDR, and differential Read/Write ports, PGL1, PGL2, PGL3, PGR1, PGR2, and PGR3. The Read Word-Line (RWL) and Virtual VSS (VVSS) are row-based, and Write Word-Line A (WWLA), Write Word-Line B (WWLB), Bit-Line (BL), and Bit-Line Bar (BLB) are column-based. The cell layout shows the layers from diffusion up to metal-3. The logic layout rules in 40GP CMOS process restrain the poly-to-poly space to several discrete spacing due to the concern of poly critical dimension uniformity (CDU) control. To comply with the design rule, we have to add 4 segments of dummy-poly in the bit-cell. Additionally, we share the dummy poly, diffusion and contacts as much as possible to minimize the bit-cell and SRAM array area. We use the minimum width for all cell transistors. The reason is that the proposed bit-cell employs Read buffers to decouple storage nodes (Q and QB) from BL and BLB to eliminate Read disturb and DAPC Write-assist to enhance Write-ability, thus there is no sizing conflict between Read and Write operations. However, we enlarge the length of PDL and PDR by 2 to reduce the leakage current of SRAM arrays to reduce static power consumption.

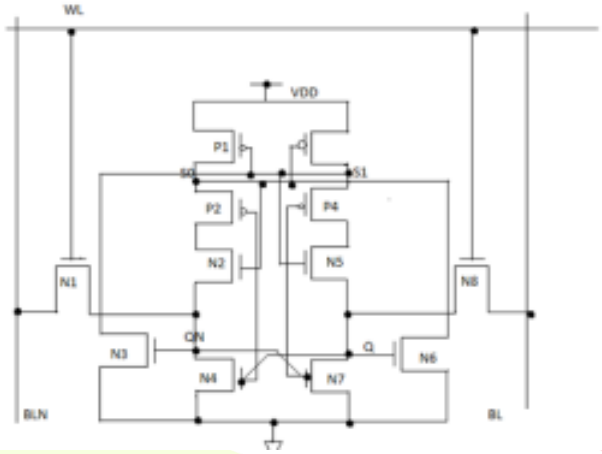

Fig.no 3: 12T SRAM cell

Read Operation With Read Buffer:

In Read mode, the selected RWL is enabled and the corresponding VVSS is forced to ground, while WWLA and WWLB remain disabled. Read buffers read the stored data to BL and BLB. Due to the differential bit-line (BL and BLB) configuration, we employ a current-mode latch sense amplifier (SA) to sense the difference of the voltages of BL and BLB for robust Read operation. To reduce the offset voltage of SA, dummy MOSs are placed adjacent to SA circuits. Since the disabled WWLA/WWLB turn on SWL/SWR and turn off PGL2/PGR2 to isolate Q and QB from BL and BLB, respectively, the Read Static Noise Margin (RSNM) of the 12T SRAM cell is almost equal to its Hold SNM and is much larger than that of 6T SRAM cell. Even though the 6T SRAM cell has been sized up by increasing the width of the pull-down NMOS transistors to mitigate Read disturb, the RSNM of the upsized 6T SRAM cell. The RSNM improvement is 4 even if 6T SRAM cell is sized up to the same area of the 12T SRAM cell. In addition, two NMOSs with minimum size are stacked in the BL/BLB to VVSS paths, thus the Read current of the 12T SRAM cell. less than that of the 6T SRAM cell. However, because the VVSSs of unselected cells sharing the same BL and BLB are held at the BL leakage of the 12T SRAM cell Therefore, a BL can afford more memory cells by using the 12T SRAM cell than the 6T SRAM cell during Read operation. Although, the 12T SRAM cell does not have Read stability problem, some peripheral Read-assist circuits can also be used to enhance Read speed without stability degradation, e.g., cascaded bit-line scheme

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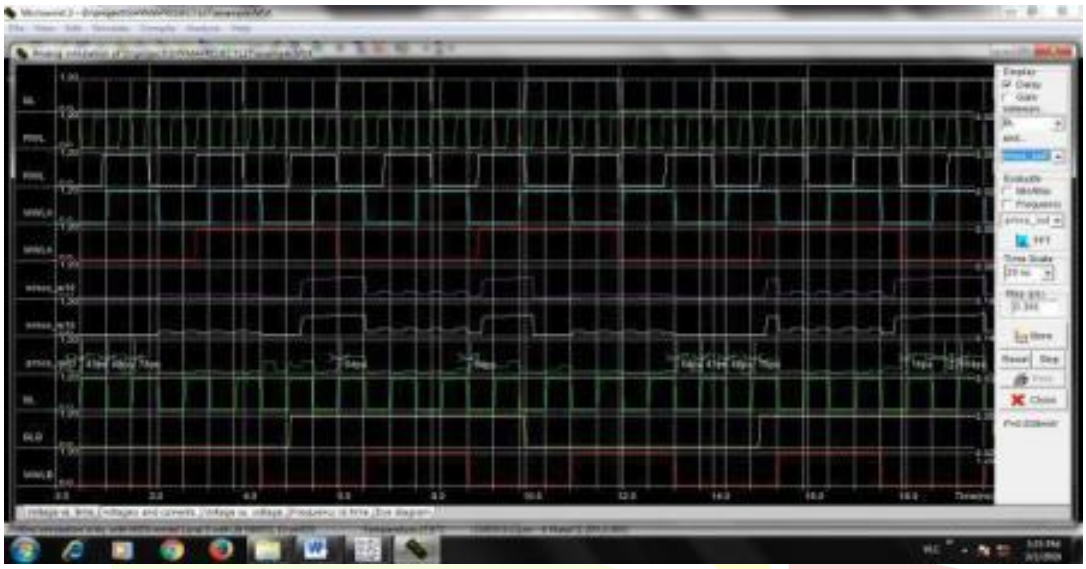

Fig.no 4(a): delay output of read operation

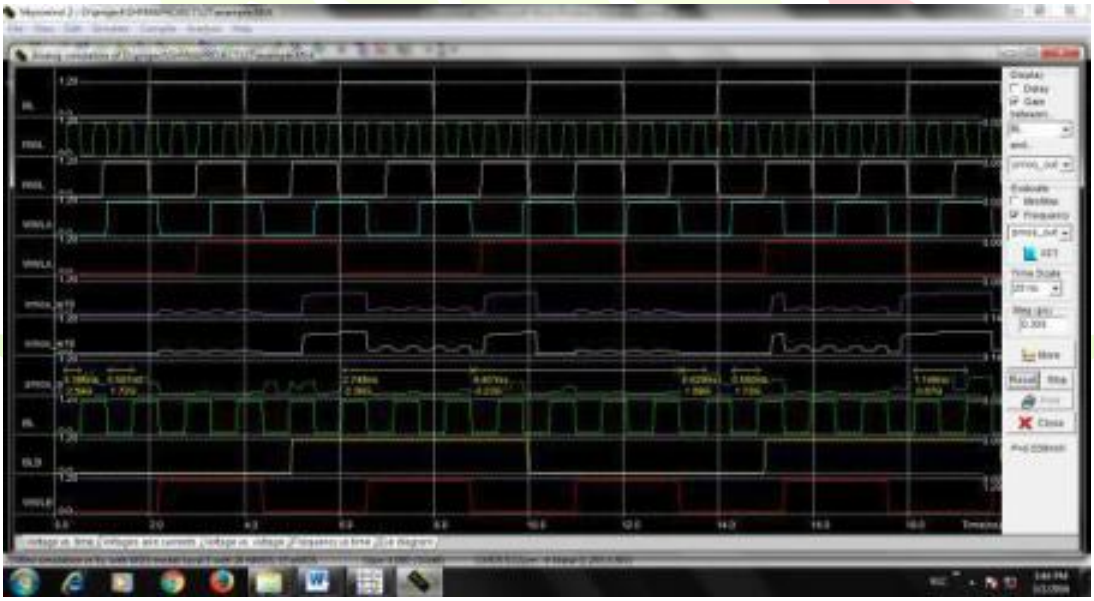

Fig.no 4(b): gain output of read operation.

Write Operation With Cross-Point Data-Aware Power-Cutoff Write-Assist (DAPC):

Illustrates the Write operation of the 12T SRAM cell with data-aware column-based WWLs. In Write "0" operation. RWL and WWLA are enabled; VVSS and BL are forced to ground; BLB is forced to while WWLB

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remains disabled. Then, node Q is discharged by BL through PGL1/PGL2 and by VVSS through PGL3 to Write "0" into the selected cell. At the same time, SWL is cut off and there is no charging path from to node Q. For Write "1" operation, RWL and WWLB are enabled; VVSS and BLB are forced to ground; BL is forced to while WWLA remains disabled. Then, node QB is discharged by BLB through PGR1/PGR2 and by VVSS through PGR3 to Write "1" into the selected cell. At the same time, SWR is cut off and there is no charging path from to node QB. Since both the row-based RWL and column-based WWLA/ WWLB need to be enabled to Write the selected cell and each column is selected individually via the values of WWLA and WWLB (i.e., Data-in), the cell provides a cross-point Write structure and there is no disturb for half-select cells during Write operation. The Write Static Noise Margin (WSNM) versus at the Slow N Fast P (SNFP) corner (the worst corner for Write) of the proposed 12T cell, the 10T cell in and the conventional 8T cell in with iso-area sized for Write operation. The proposed 12T cell has the best WSNM due to the DAPC Write-assist scheme.

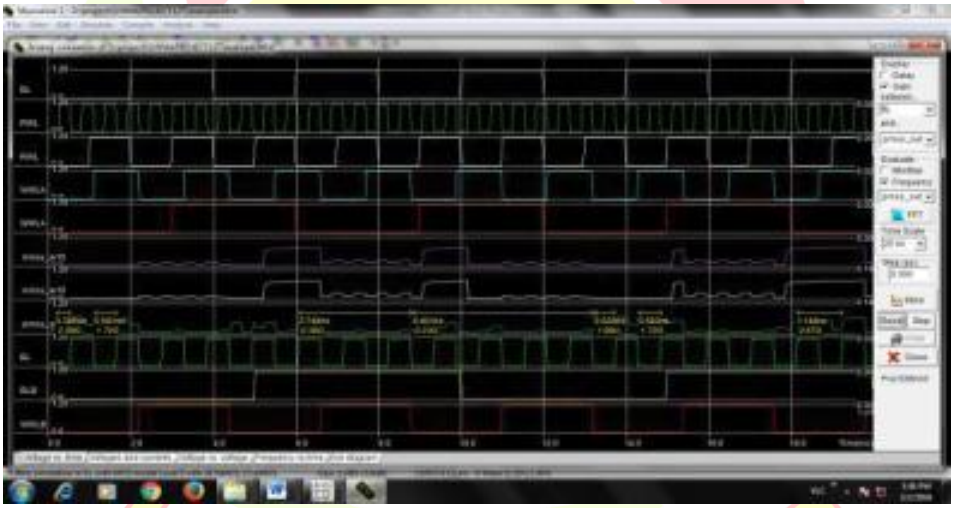

Fig.no 5(a): gain output of write operation

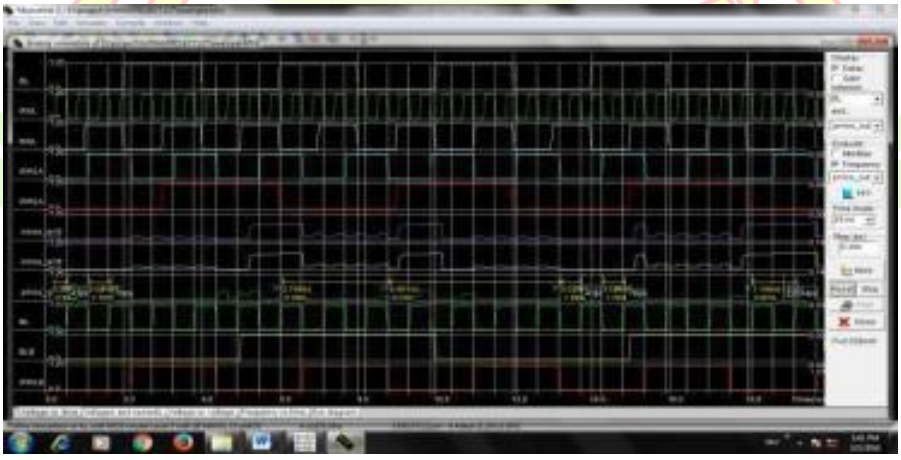

Fig.no 5(b): delay output of write operation.

ADVANTAGES:

- It reduces the power dissipation.
- It also gives the lower power delay product and energy delay products.

APPLICATION:

- All memory circuits.
- Biomedical applications.
- Digital circuits memory applications.

CONCLUSION:

A bit-interleaving 12T sub threshold SRAM cell with data aware power-cutoff Write-assist has been demonstrated in this method. The 12T cell eliminates Read disturb and Write half select disturb, and improves the Write-ability by using data aware power-cutoff scheme for robust sub threshold operation. Low-voltage operation is accomplished without the need for any additional peripheral Write- and Read-assist circuits. The measured results demonstrate error free functionality under the worst-case bit-line data patterns down, voltage), limited by Read operation. Data can be written successfully, In sub threshold region, chip operates power consumption. The minimum energy per operation.

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