DESIGN AND COMPARISON OF 128*128 VEDIC MULTIPLIER USING CADENCE

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Abstract – The prerequisite of great speed multiplier is increasing as the need of increasing high speed processors. A multiplier is one of the hardware blocks in fastest processing system. This is not only a high delay block but also a major source of power dissipation. A conventional processor necessitates substantially more hardware resources and more processing time in the multiplication operation sooner than addition and subtraction. In this project, we implement a high speed multiplier using algorithm stated in Indian ancient Vedic mathematics which is utilized for all case of multiplication and to progress the enactment of multiplier. In this method, as the number of multiplier bits increases it requires less number of calculations relate to other existing multiplication Algorithm. In this paper the Vedic multiplier is compared with the current method such as booth and array multiplier. The Vedic multiplier is designed using Urdhva sutras. This algorithm shrinks the overall delay of the multiplier unit.The computational path delay for proposed 128x128 bit Vedic multiplier is found to be 211.554 ns

Keywords-Ripple carry (RC) Adder, Multiplication, Vedic Mathematics, Vedic Multiplier (VM), UrdhvaTriyakbyham Sutra.

1. INTRODUCTION

Multipliers are widely recycled in microprocessors, DSP and communication applications. For higher order multiplications, a vast number of adders are to be user to perform the partial product addition. The need of high speed multiplier is aggregate as the prerequisite of high speed processors are swelling. Advanced throughput arithmetic operations are important to achieve the anticipated performance in many real time signal and image processing applications. One of the crucial arithmetic operations in such solicitations is multiplication and the enlargement of fast multiplier circuit has been a subject of interest over spans. Tumbling the time delay and power consumption are very crucial requirements for many applications**.** In the bygone multiplication was fulfilled normally with a sequence of addition, subtraction and shift operations. Two furthermost common multiplication algorithms tracked in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. Owing to the prominence of digital multipliers in DSP, it has always been a research. Vedic mathematics is the forename set to the early system of mathematics, which was revived from the ancient Indian scriptures flanked in 1911 to 1918 byJagadguru Swami Sri BharatiKrishaTirthaji (1884-1960), a logical of Sanskrit, mathematics, history and philosophy. The unabridged of Vedic mathematics is based on 16 Vedic sutras, which are actually word prescriptions recitation natural ways of cracking an unabridged range of mathematical problems [1]. The paper is organized as surveys. Section II graces the elementary methodology of Vedic multiplication technique. Section III describes the anticipated multiplier architecture centered on Vedic multiplication and the generalized algorithm for N*N bit Vedic multiplier. Section IV designates the scheme and implementation of Vedic multiplier module in XilinxISE12.1. Section V comprises of Outcome and Discussion in which device utilization summary besides computational path delay proficient for the anticipated Vedic multiplier (after synthesis) is argued. As a final point, Section VI comprises of Conclusion.

2.VEDIC MULTIPLICATION TECHNIQUE

The routine of Vedic mathematics deceptions in the fact that it shrinks the typical calculations in conventional mathematics to alike meek one. This is so for the cause that the Vedic formulae are claimed to be centered on the natural doctrines on which the human mind works. Vedic Mathematics is a style of arithmetic rubrics that allow further efficient speed implementation. It also affords some nominal algorithms which can be applied to various branches of engineering such as computing.

2.1 URDHVA TRIYAKBYHAM SUTRA

The anticipated Vedic multiplier is based on the "UrdhvaTiryagbhyam" sutra (algorithm). These Sutras have been traditionally recycled for themultiplication of two numbers in the decimal number system. In this effort, we apply the same ideas to the binary number system to sort the anticipatedalgorithm compatible with the digital hardware. It is an overall multiplication prescription applicable to all from side to side which the cohort of all partial products can be done with the coexisting gears of multiplication. It factually means "*Vertically and Crosswise*". It is positioned on a well-worn notionally of these partial products. The algorithm can be comprehensive for n x n bit number. Meanwhile the partial products and their sums are calculated in analogous, the multiplier is sovereign of the clock frequency of the processor. Due to its regular structure, it can be certainly blueprint in microprocessors and designers can easily evade these problems to avoid catastrophic device failures. The dispensation power of multiplier can easily be augmented by increasing the input and output data bus widths since it has a fairly an unvarying structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier centered on this sutra has the pro that as the number of bits' increases, gate delay and area increases very sluggishly as compared to further conventional multipliers.

2.2 Multiplication of two decimal numbers 252 * 846

To elucidate this structure, let us cogitate the multiplication of two decimal numbers 252 * 846 by Urdhva-Tiryakbhyam method as shown in Fig. 1. The cyphers on the equally sides of the line are multiplied and added with the carry from the previous pace. This engenders unique bits of the result and a carry. This carry is added in the next step and hence the course goes on. If above one line is there in one step, all the results are added to the previous carry. In each stage, least significant bit turns as the result bit and all other bits turns as carry for the next step. Primarily the carry is taken to be zero.

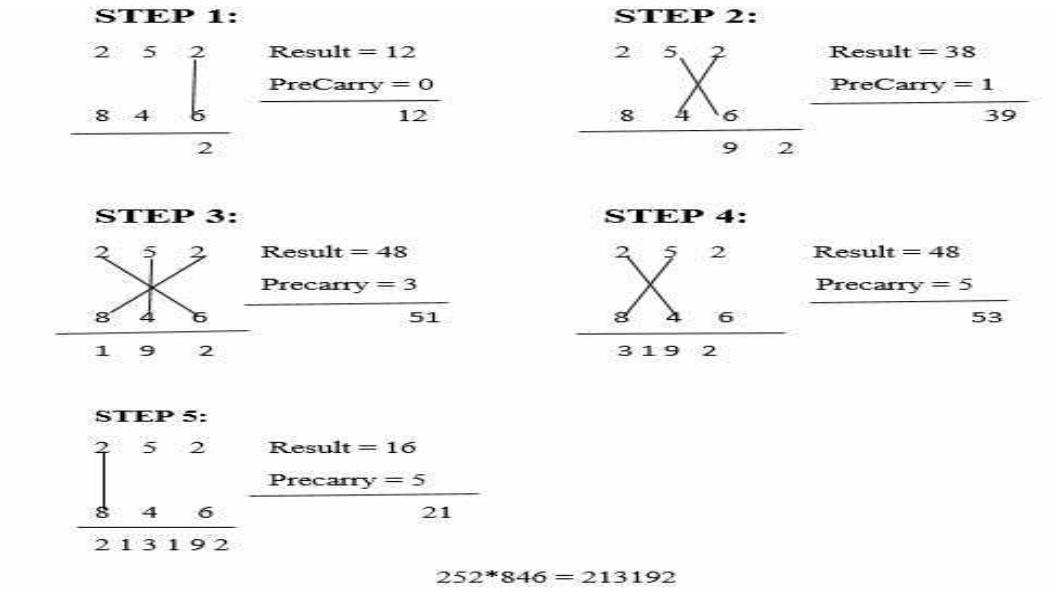

Figure 1: Multiplication of 256*846

3. THE PROPOSED MULTIPLIER ARCHITECTURE

The magnificence of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is The hardware architecture of 2*2, 4*4 and 8*8-bit Vedic multiplier module are displayed in the below sections. At this juncture, "Urdhva-Tiryagbhyam" (*Vertically and Crosswise*) sutra is recycled to propose such architecture for the multiplication of two binary numbers well adapted to parallel processing. The feature makes it

more attractive for binary multiplications. This in crack shrinks delay, which is the primary motivation behind this work.

3.1 Vedic Multiplier for 2*2-bit module

The scheme is designated below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Fig. 2. Firstly, the least significant bits are multiplied which springs the least significant bit of the final product (vertical). Formerly, the LSB of the multiplicand is multiplied with the succeeding higher bit of the multiplier and added with, the product of LSB of multiplier and succeeding higher bit of the multiplicand (crosswise). The sum springs second bit of the final product and the carry is added by means of the partial product gained by multiplying the most significant bits to give the sum and carry. The sum is the third analogous bit and carry becomes the fourth bit of the final product.

$s0 = a0b0;$ (1)

$c1s1 = a1b0 + a0b1;$ (2)

$c2s2 = c1 + a1b1;$ (3)

The ultimate result will be *c*2*s*2*s*1*s*0. This multiplication routine is applicable for all the gears.

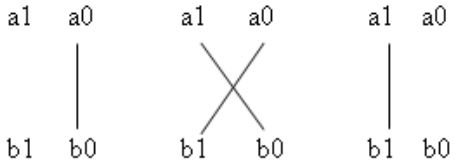

Figure 2: The Vedic Multiplication Method for two 2-bit Binary Numbers

The 2*2 Vedic multiplier segment is implemented via four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It initiate that the hardware design of 2*2-bit Vedic multiplieris similar as the hardware design of 2*2-bit conventional Array Multiplier [2]. Later it is determined that multiplication of 2 bit binary numbers by Vedic method does not made major upshot in improvement of the multiplier's efficiency. Self-same precisely we can state that the aggregate delay is only 2-half adder delays, after ultimate bit products are engendered, which is very similar to Array multiplier. So we barter to the enactment of 4*4-bit Vedic multiplier which uses the 2*2-bit multiplier as an elementary building block. The same routine can be extended for input bits 4 & 8. But for greater no. of bits in input, slight modification is required.

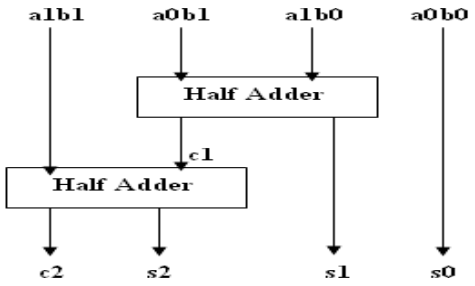

Figure 3: Block Diagram of 2*2 – bit Vedic Multiplier

3.2 Vedic Multiplier for 4x4 bit Module

The 4*4- bit Vedic multiplier segment is implemented using four 2*2- bit Vedic multiplier modules as argued in Fig. 3. Let's scrutinize 4*4 multiplications, say A= A3 A2 A1 A0 and B= B3 B2 B1 B0. The output line for the multiplication upshot is – S7 S6S5S4 S3 S2 S1 S0. Let's divide A and B into two parts, say A3 A2 & A1 A0

for A and B3 B2 & B1B0 for B. Consuming the vital of Vedic multiplication, taking two bit at a time and using 2-bit multiplier block, we can have the ensuing structure for multiplication as shown in Fig. 4. fundamental of Vedic multiplication, taking two bit at a time and via 2-bit multiplier block, we can have the succeeding structure for multiplication as shown in Fig. 4.

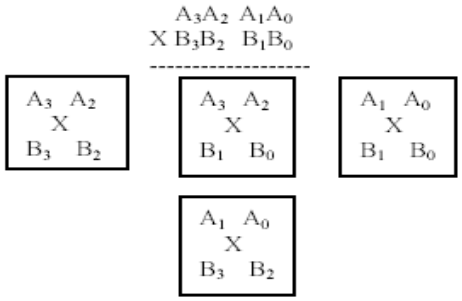

Figure 4: Sample Presentation for 4*4-bit Vedic Multiplication

Each slab as presented above is 2*2-bit Vedic multiplier. First 2*2-bit multiplier inputs are A1A0 and B1B0. The last slab is 2*2-bit multiplier with inputs A3 A2 and B3 B2. The middle one shows two 2x2 bit multiplier with inputs A3 A2 & B1B0 and A1A0 & B3 B2. So the ultimate upshot of multiplication, which is of 8 bit, S7 S6S5S4 S3 S2 S1 S0. To understand the conception, the Block diagram of 4*4-bit Vedic multiplier is shown in Fig. 5. To acquire ultimate artifact (S7 S6 S5 S4 S3 S2 S1 S0), four 2*2-bit Vedic multiplier (Fig. 3) and three 4-bit Ripple-Carry (RC) Adders are required. The proposed Vedic multiplier can be used to shrink delay. Timely fiction speaks about Vedic multipliers based on array multiplier structures. Contrariwise, we proposed a new architecture, which is efficient in terms of speed. The arrangements of RC Adders shown in Fig. 5, helps us to shrink delay. Interestingly, 8*8 Vedic multiplier modules are implemented easily by using four 4*4 multiplier modules.

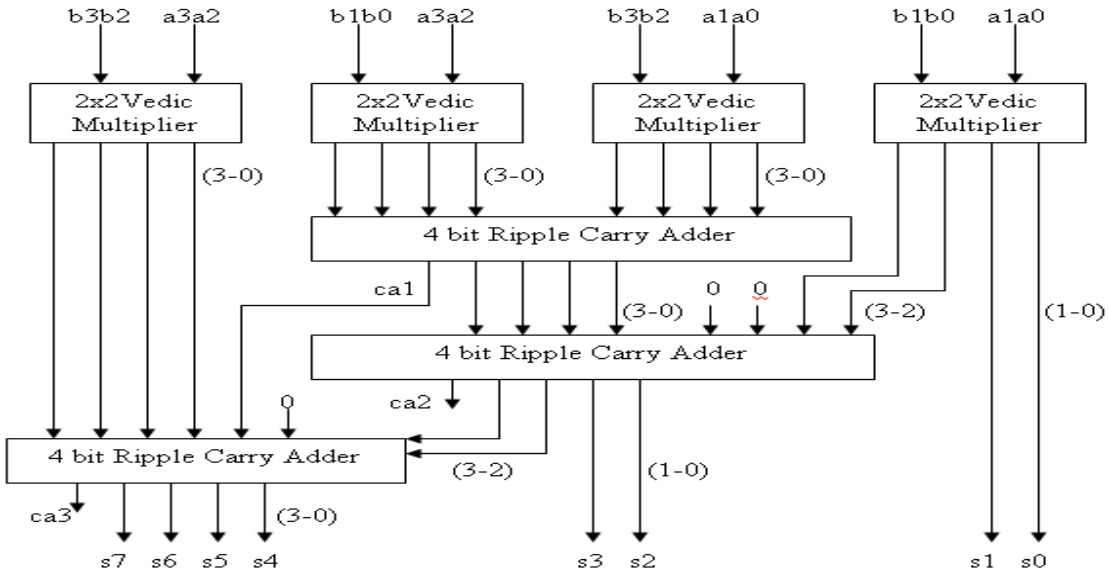

Figure 5: Block Diagram of 4*4 – bit Vedic Multiplier

$$P = A \times B = (AH\text{-}AL) \times (BH\text{-}BL)$$
$$= AH \times BH + (AH \times BL + AL \times BH) + AL \times BL$$

Expending the vital of Vedic multiplication, taking four bits at a time and via 4-bit multiplier block as argued we can accomplish the multiplication. The outputs of 4*4 -bit multipliers are added consequently to gain the ultimate product. At this juncture aggregate three 8-bit Ripple-Carry Adders are required as shown in Fig. 6.

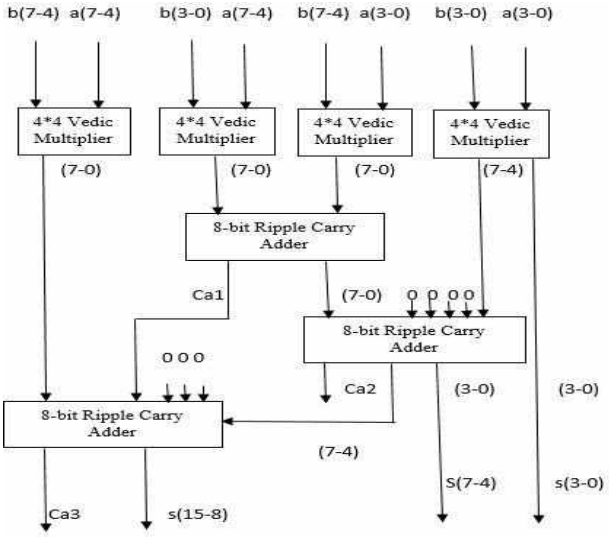

Figure 6: Block Diagram of 8*8-bit Vedic Multiplier

3.4 Vedic Multiplier for 128*128 – bit Module

The 64*64 - bit Vedic multiplier module as shown in the lump diagram in Fig. 7 can be easily implemented by using four 64*64 -bit Vedic multiplier modules as discussed in the previous slice. As shown in the Figure 5.1.7 128*128 -bit Multiplier can be designed with four 64*64-bit multiplier blocks and the adder used in the architecture is 128 bit ripple carry adder.

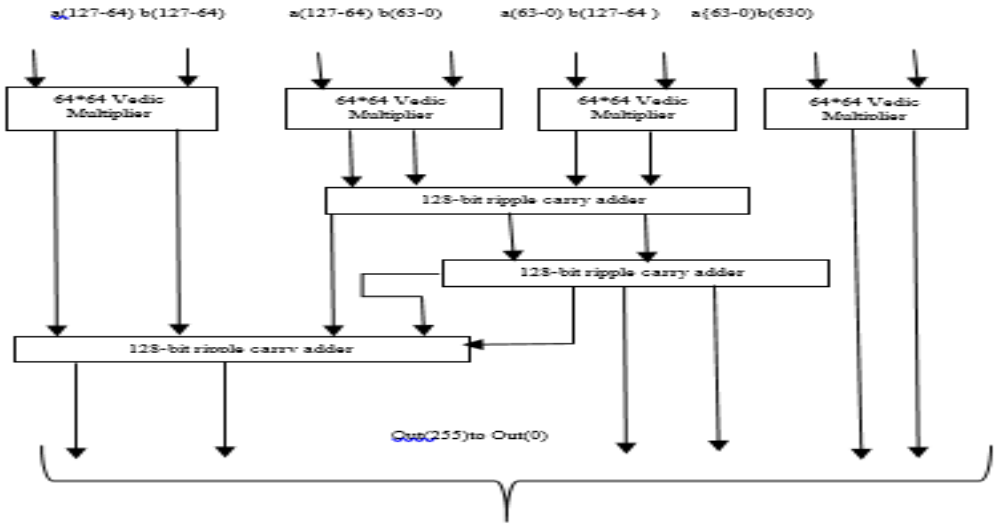

Figure.7 Block Diagram of 128*128 bit Urdhva Multiplier

3.5 Generalized Algorithm for N * N bit Vedic Multiplier

We can oversimplify the routine as argued in the prior slices for any number of bits in input. Let, the multiplication of twofold N-bit binary numbers (where N = 1, 2, 3…N, must be in the form of 2N) *A* and *B* where A

= AN.....A3 A2 A1 and B = BN…. B3 B2 B1. The ultimate multiplication upshot will be of (N + N) bits as S = S (N + N) .... S3 S2 S1.

Step 1: Fragmented the multiplicand A and multiplier B into two equivalent parts, each consisting of [N to (N/2) +1] bits and [N/2 to 1] bits correspondingly, where first slice signposts the MSB and other represents LSB.

Step 2: Signify the parts of A as AM and AL, and slices of B as BM and BL. Now represent A and B as AM AL and BM BL separately.

Step 3: For A X B, we have general format as shown in Fig.

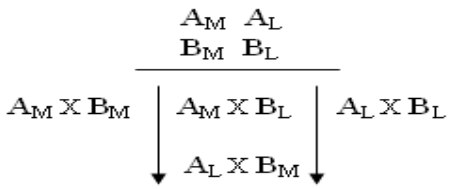

Figure 8: General Representation for Vedic Multiplication

Step 4: The individual multiplications product can be gained by the partitioning routine and applying the basic building blocks.

By espousing the above sweeping algorithm, we can utensil Vedic Multiplier for any number of bits' say16, 32, 64, and so on, as per the prerequisite. Therefore, it could be probable to utensil this Vedic multiplier in the ALU (Arithmetic Logic Unit) which will shrink the computational speed hugely & hence improves the processors efficiency

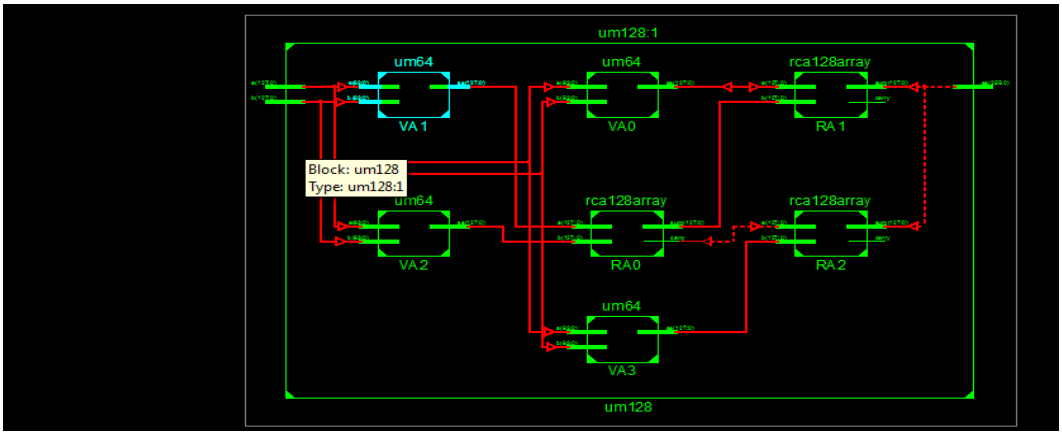

Figure 9. RTL Schematic of 128*128-bit Vedic Multiplier

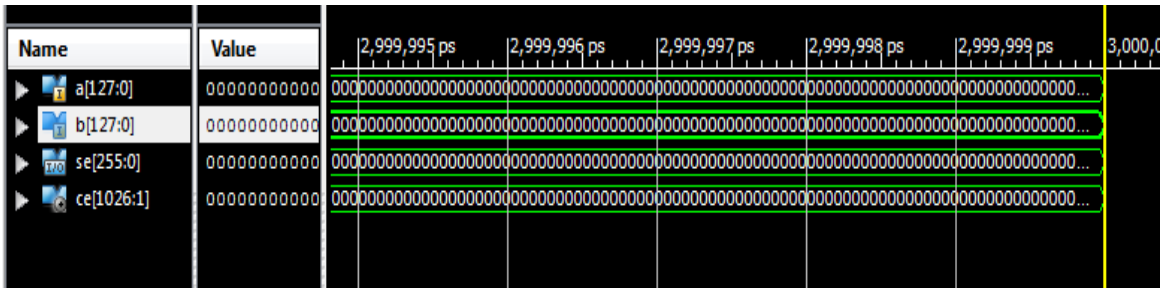

Figure 10. Simulation Result of 128*128 – bit Vedic Multiplier

Table 1. Device Utilization summary (Estimated values)

Logic Utilization	Used	Available	Utilization
No.Of Slices	29424	768	463%
No.Of 4 i/p LUTs	51923	1536	460%
No .Of Bounded IOBS	512	124	363%

4. RESULT AND DISCUSSION

The synthesis result gained from anticipated Vedic multiplier is sooner than Array and Booth multiplier. The device utilization summary of 8*8-bit Vedic multiplier for Xilinx, Spartan family is exposed below: Table 2 spectacles the comparison of 8*8 bit Conventional multipliers with Vedic multiplier (ours) in terms of computational path delay in nanoseconds (ns). The path delay for 8*8-bit Array and Booth multipliers have been taken from S.S. Kerur et al. [7]. The timing result shows that Vedic multiplier has the utmost pro as compared to other multipliers in terms of execution time.

Table 2. Delay Comparison Table

Device	Booth Multiplier		Array Multiplier		Urdhva	
xc3s250epq208-5	4*4	8*8	4*4	8*8	4*4	8*8
Path Delay	15.34 ns	44.57ns	13.14ns	33.74 ns	12.74ns	21.57 ns

4.1 DEVICE UTILIZATION COMPARISION

The amalgamation upshot gained from proposed Vedic multiplier is sooner than Array and Booth multiplier. The device utilization summary of 8*8-bit Vedic multiplier for Xilinx, Spartan family is exposed below: Table 3 shows the device utilization comparison of 8*8 –bit Vedic multiplier

Table 3. Device Utilization Comparison Table

Device	Booth Multiplier		Array Multiplier		Urdhva Multiplier	
xc3s250epq208-5	4*4	8*8	4*4	8*8	4*4	8*8
No of Slices	27 out of 960	38 out of 960	33 out of 960	119 out of 960	18 out of 960	93 out of 960
No of 4 i/p LUTs	49 out of 1920	124 out of 1920	33 Out Of 1920	234 Out Of 1920	32 Out Of 1920	165 Out Of 1920
No of Bonded IOBs	16 out Of 66	32 Out Of 66	16 Out Of 66	32 Out Of 66	16 Out Of 66	32 Out Of 66

5. CONCULSION

This paper boon a vastly efficient method of multiplication – "UrdhvaTiryakbhyam Sutra" erected on Vedic mathematics. It springs us monotonous for hierarchical multiplier design and clearly signposts the computational pro offered by Vedic methods. The computational path delay for proposed 128x128 bit Vedic multiplier is found to be 211.554 ns. Hence our motivation to shrink delay is excessively fulfilled. Therefore, we observed that the Vedic multiplier is much more proficient than Array and Booth multiplier in relations of execution time (speed). An awareness of Vedic mathematics can be effectively enlarged if it is included in engineering education. In imminent, allthe major universities may set up apposite research centers to promote research works in Vedic mathematics.

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