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DESIGN AND ANALYSIS OF MULTIPLIER USING REVERSIBLE LOGIC GATES

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ABSTRACT: Reversible logic due to its reduced power consumption has captured substantial digital logic design. Its salient features are recovering from bit loss and unique input output mapping where conventional logic failed. The low power multiplier has been designed by using various reversible gates. By using these reversible gate analysis of parameters such as area, power, delay, and garbage output can be done. This work proposes a novel 8 × 8 bit reversible fault tolerance multiplier circuit which can multiply two 8 bit numbers. This was based on two concepts the partial product that can be generated in parallel using peres gate. However, the addition is done by using reversible parallel adder designed from TSG gate, Feyman gate, Toffoli gate, MFA gate and comparison had been taken between these gates**.**

Keywords: TSG gate, MFA gate, Peres gate.

I INTRODUCTION

Energy dissipation is a vital contemplation in VLSI design. Reversible logic associates the energy with Landauer circumstances that information loss was predominantly due to utility irreversibility prominent to energy dissipation. Various logic gates and its applicability on logic design had been discussed by [Mamataj, Set all] extravagantly which finds its presentation in considerable calculating, low power CMOS, DNA calculating, digital signal processing (DSP), quantum dot cellular mechanisms etc. The loss of each information bit is KT × ln2 joules of energy, somewhere Boltzmann constant is denoted as K and T is the temperature at which the system is operative.

II RELATED WORKS

A. Application in logic design

Reversible logic has become one of the most hopeful research areas in the supporters few decades and has found its presentations in numerous technologies; such as low power CMOS, nanotechnology and optical computing. The main purposes of deceitful reversible logic are to Diminutions quantum cost, depth of the circuits and the number of garbage harvests.The purpose of this tabloid is to give a mount of reference, empathetic and indication of reversible gates**.** In this tabloid innumerable logic gates and its application on lucidity design have been discussed. Also a brief framework of comparisons between various reversible circuits is unfilled on the basis of various constraints. The revocable courses form the basic edifice tablet of considerable mainframes. This paper grants the embryonic reversible gates which are congregated from prose and this paper helps scholars/designers in designing higher complex computing circuits using reversible gates. The tabloid can auxiliary be prolonged towards the digital design evolution using reversible logic tracks which are helpful in quantum calculating, low power CMOS, nanotechnology, cryptography, optical computing, DNA calculating, digital signal processing(DSP), quantum dot cellular mechanisms, communication, workstation illustrations.

B. Reversible TSG Gate

In the current an inordinate length of time, reversible logic has occurred as a auspicious technology having its applications in low power CMOS, quantum computing, nanotechnology, and optical computing. The predictable set of gates such as AND, OR, and EXOR are not reversible. In recent times a 4*4 reversible gate called "TSG" is projected. The most substantial aspect of the projected gate is that it can work piecemeal as a reversible full adder, that is reversible full adder can now be employed with a single gate only. This tabloid proposes a NXN reversible multiplier using TSG gate. It is grounded on two concepts. The limited vintages can be generated in parallel with a adjournment of using Fredkin gates and thereafter the addition can be reduced to log N steps by using reversible parallel adder designed from TSG gates. A 4x4 architecture of the projected reversible multiplier is also designed. It is demonstrated that the proposed multiplier architecture using the TSG gate is much better and enhanced,compared to its remaining counterparts in literature; trendyterms of number of reversible gates and garbage outputs. Thus, this tabloid provides the preliminary threshold to building of more complex system which can accomplish more byzantine operations using reversible logic. The focus of this paper is the tender of the freshly proposed reversible 4*4 TSG gate. A NXN reversible multiplier is also proposed in this paper. It isproved that the proposed multiplier planning usingthe projected TSG gate is better than the prevailingcounterpart in prose in terms of reversible gates and garbage outputs. All the proposed architectures are investigated in terms of technology sovereign implementations. The technology independent analysis is requisite since quantum or optical logic executions are not available. There are a number of noteworthy applications of reversible logics such as low power CMOS, quantum computing, nanotechnology, and optical computing and the proposed TSG gate and competent multiplier architecture are one of the assistances to reversible logic. Thus this, broadside provides the initial threshold to build more complex systems which can which can

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execute more intricate operations. The reversible circuits designed and proposed here for the basis of the ALU of a primitive quantum CPU.

C. Reversible Signed Multiplier

Supremacy saving circuits are the prerequisite of the modern technology which can be accomplished by using reversible logic. In this tabloid, we proposition an efficient design of a reversible n × n retained multiplier circuit, where n is the number of bits of each operand of the multiplier. We proposition a novel architecture of a general reversible compressor to reduce the number of partial products. Two algorithms have been offered to construct the Partial Product Generation (PPG) circuit and the Multi Operand Addition (MOA) circuit of the projected multiplier. Our proposed design of MOA circuit needs only two steps to get the final output which is much augmented than existing Wallace Tree multiplier. During the recognition process of the multiplier, two new gates have been proposed named as LS gate and LN gate to speed up the group of partial products. The qualified study shows that our proposed design is much better than the prevailing approaches in terms of numbers of gates, garbage outputs, quantum cost and delay. This rag presented the design methodology of an efficient and sweeping reversible multiplier which works both for signed and unsigned binary numbers. The PPG and MOA circuits are grasped by two algorithms which make the multiplication nearer by reducing number of levels or steps. An estimate between existing and projected works has been presented in terms of different cost constraints to show the improvement of the projected work. The replication verifies that our projected design works correctly. Our proposed reversible signed multiplier can be used in arithmetic logic unit which can be additional used to design a reversible processor for quantum computer.

D. Synthesizing Multiplier in Reversible Logic

Formerly, reversible logic has become an penetratingly intentional research topic. This is mainly encouraged by its submissions in the domain of low-power proposal and quantum computation. Since reversible logic is subject to certain restrictions (e.g. fan out and feedback are not allowed), traditional synthesis methods are not applicable and specific methods have been developed. In this tabloid, we focus on synthesis of multiplier circuits in reversible logic. Three methods are obtainable that report the shortcomings of former approaches. In particular, the large number of circuit lines in the resulting realizations as well as the poor scalability. Finally, we compare the results to circuits obtained by general purpose synthesis approaches. In this tabloid, we introduced three methods for multiplier synthesis that particularly address the drawbacks of previous approaches (e.g. the large number of circuit lines in the resulting realizations as well as the poor scalability). We showed that multiplier with a lower number of circuit lines can be obtained by using an adjusted specification of the underlying function. Besides that, two constructive approaches for synthesis of multipliers with very large bit-width are proposed. Experiments confirmed that using these methods, multipliers with large bit-widths can efficiently be synthesized, while previous approaches as well as universal perseverance amalgamation schemes do not scale very well on multiplication.

III BASIC DEFINITIONS

Feynman gate is a 2*2 one complete reversible gate as exposed in figure 3.1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are demarcated by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate

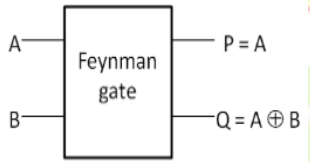

Figure 3.1 Feynman gate

Since a fan-out is not tolerable in reversible logic, this postern is useful for replication of the required outputs.

The 3*3 Toffoli gate which is publicised in the symbol 3.2 has the participation vector I (A, B, C) and the output vector is O(P,Q,R). The outputs are definite by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

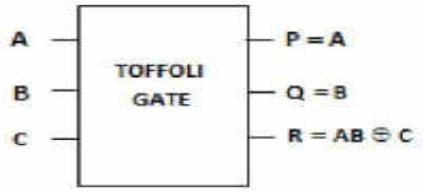

Figure 3.2 Toffoli gate

The 3*3 Fredkin gate which is pronounced in the symbol 3.3 has input vector I (A, B, C) and the output vector is O(P, Q, R). The output is demarcated by P=A, Q=A′B⊕AC and R=A′C⊕AB. Considerable total of a Fredkin gate is 5.

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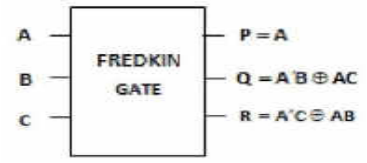

Figure 3.3 Fredkin gate

GARBAGE OUTPUTS

Annoying or unexploited output of a reversible gate (or circuit) is branded as garbage output, that is, the productivity(s)which is (are) required only to continue the reversibility is (are) known as garbageproductivity(s). Heavy price is paid off for each garbage output. The illustration for garbage outputs is given beneath where g1 and g2 are garbage harvests

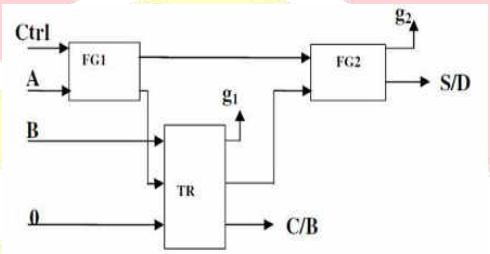

Figure 3.5 Garbage outputs

QUANTUM COST

The considerable rate can be consequential by replacing the reversible gates of a course by a cataract of uncomplicated quantum gates. Rudimentary quantum gates recognise quantum circuits that are innately reversible and deploy qubits rather than pure logic values. The state of a qubit for two uncorrupted logic states can be expressed as $|c\rangle = \alpha|0\rangle + \beta|1\rangle$, where $|0\rangle$ and $|1\rangle$ represent 0 and 1, respectively, and α and β are the complex numbers such that $|\alpha|2 + |\beta|2 = 1$. The most used uncomplicated quantum gates are the NOT gate (a single qubit is inverted), the CNOT gate (the target qubit is reversed if the single control qubit is 1), the controlled-V gate (also known as a square root of NOT, since two following V operations are equivalent to an inversion), and the controlled-V + gate (which performs the inverse operation of the V gate and thus is also a square root of NOT).

AREA

The extent of a logic journey is the addition of detached area of respectively gate of the circuit. If a reversible circuit consist of n reversible gates and the extent contains (a_1, a_2, ..., a_n). The area (A) of circuit is

$$A = \sum_{i=1}^{n} (a_i)$$

The area of a circuit can be considered easily by locating extent of respectively distinct gate consuming CMOS 90nm Cadence Design Systems.

POWER

The supremacy of a logic course is the addition of detached power of each opening of the circuit. If a reversible course consist of n reversible gates andthe power contains (p_1, p_2, ...,p_n). The extent (P) of track is

$$P = \sum_{i=1}^{n} (p_i)$$

The supremacy of a circuit can be measured easily by gaining power of each individual postern consuming CMOS 90nm Cadence Design Systems.

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IV RESULTS AND DISCUSSION

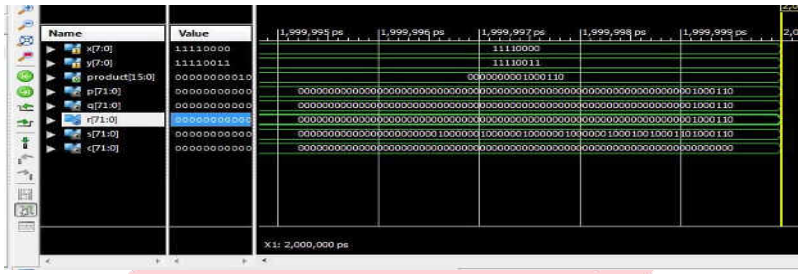

Figure 1 Feynman output

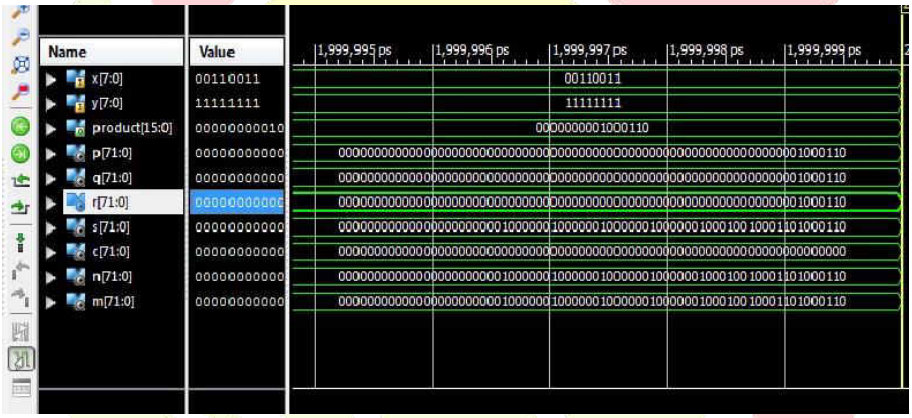

Figure 2 TSG output

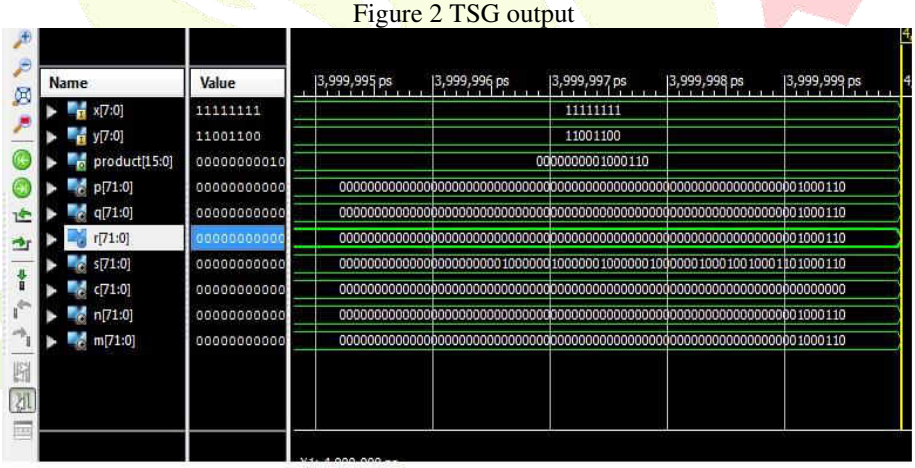

Figure 3 MFA output

Figure 4 Peres output

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Performance Analysis

Parameter	PERES	MFA	FG&TG	TSG
Power	184	169	180	179
Area	19780	15365	13037	18718
Delay	27.868ns	26.289ns	27.85ns	27.85ns

Table 1 shows the performance analysis of reversible gates

When compared to the existing method, the proposed design produces good result and the performance inquiry is calculated using cadence tool.

V CONCLUSIONS

The existing method consists of 4*4 reversible multiplier concepts which include partial product generation and full adder. In the existing method Peres gate is used for both partial product generation and full adder. Therefore the proposed method consists of 8*8 multiplier circuit which include various gates such as Feynman gate, MFA gate, Peres gate, TSG gate, Tofolli gate for partial product generation and full adder. By comparing these gates we have analysed parameters such as Area, Power, Delay. Further I have planned to design a multiplier accumulator unit MAC based on these reversible logic gates.

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