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LOW POWER SERIAL DIVIDER USING MOD-GDI TECHNIQUE

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***Abstract*—** Divider is a basic hardware module in advanced and high speed digital signal processing (DSP) units. It has the applications in radar technology, communication, industrial control systems and linear predictive coding (LPC) algorithms in speech processing. This paper presents 4-bit Serial Divider using Modified GDI Technique. The repeated one's complement method of binary subtraction algorithm is used for serial division. The proposed method aims on Modified Gate Diffusion Input (mod-GDI) which is a low power technique to design any digital system. This technique has been adopted from Gate Diffusion Input (GDI).The Modified GDI technique which allows in reducing delay, power consumption and area compared to conventional CMOS Technology. According to the estimations done, the transistor count, Tool analysis time, power consumption of serial divider using CMOS technology and the Modified GDI technique is tabulated. The designs are simulated using the Tanner EDA tool.

Keywords— GDI, Modified-GDI, Transistor Count, Power Consumption, One's Complement Method of Subtraction.

Introduction

Digital systems have such a prominent role in everyday life that we refer to the present technological period as the digital age. Digital systems are used in communication, business transactions, traffic control, space guidance, medical treatment, weather monitoring and scientific enterprises. With many applications needs support for arithmetic units, complex arithmetic modules like multipliers and dividers are now being extensively used in digital design. Here the serial division using the modified GDI technique is introduced. Division[7] is a fundamental function in the digital systems. Binary divider can be classified in two types, serial divider and parallel divider. The operation of serial division[5] can be done by means of repeated subtraction. Suppose we want to divide 18 by 3. So we repeatedly subtract 3 from 18 and after six times subtraction, remainder is zero so less than the divisor, then further subtraction is stopped. So the quotient comes out as six and the remainder as zero.

The serial divider consists of 4-bit binary adder[6], 2:1 multiplexer[8], 4-bit synchronous up counter, negative edge triggered Master Slave D flip flop. Here the 4-bit carry-lookahead adder is used for the fast addition process. Divider circuits are the main building blocks of the Arithmetic unit. Hence the certain parameters like power, area, delay time to be considered. To reduce the area and power various techniques are used. Some of them are CMOS, Transmission Gate [1], Pass Transistor logic [1] etc. Although these several techniques have been proposed to reduce the area, power consumption but there were some limitations like low logic level and circuit complexity in it. This paper presents the modified GDI technique to overcome these limitations. The proposed 4-bit binary serial divider is implemented using Tanner EDA Tool. This tool provides sophisticated capabilities with high speed and ease of design.

II. BACKGROUND

. The method of binary division of binary number 1101(decimal 13) by binary number 0100(decimal 4) by One's complement method of subtraction is shown in Fig.1.This operation is followed in the serial divider circuit.

Step: 1
1101(13)
+1011(ones complement of 4)
11000
→ 1
1001(9)

step: 2
1001(9)
+1011
10100
→1
0101(5)

Step: 3
0101(5)
+1011
10000
→ 1
0001(1)

step: 4
0001(1)
+1011
01100
↓ -0011(-3)
carry is zero

Fig.1.One's complement method of subtraction

Here when difference is positive final carry is 1 which is end around and added to get the actual difference. When difference is negative, carry is zero and true result is obtained by one's complement of the sum output.[5] so here we have to perform the repeated subtraction till final carry 1.since subtraction is for three times, when carry is 1, so quotient will be 3 and remainder is final difference, which is 0001.

I. PROPOSED WORK

The serial divider is already implemented by using the transmission gate technology[5]. In this paper we implement the serial divider using the modified GDI technique. The implementation of 4-bit binary serial divider by means of repeated subtraction of two 4-bit binary numbers is shown in Fig.2.Here the divisor Y3Y2Y1Y0 is subtracted from X3X2X1X0 by one's complemented method of subtraction.
The basic building blocks used are,
1) Adder.

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2) 4-bit binary synchronous up counter.
3) 2:1 Multiplexer.
4) Master Slave D flip-flops.

Each bit of divisor is inverted and fed to 4 bit binary adder inputs. Dividend is initially loaded in a register comprising of four D flip-flops by putting load input high, which is common select input of all the multiplexer [8] and also to the clear input of the counter. Initially, counter is also reset to zero. Output of the D flip-flops is fed to another set of inputs of adder. The final carry output of the adder block is fed into the clock enable input of the counter and also to an OR gate. Its other input is LOAD and output goes to clock enable of register. We assume that divisor (Y) and dividend (X) are non-zero numbers and X > Y, we shall have carry output of adder high initially since we are adding X with one's complement of Y. For one's complement method of subtraction there should be an end around carry. Here we are interested till there is a carry output in the adder and hence the carry input of the adder is tied high.

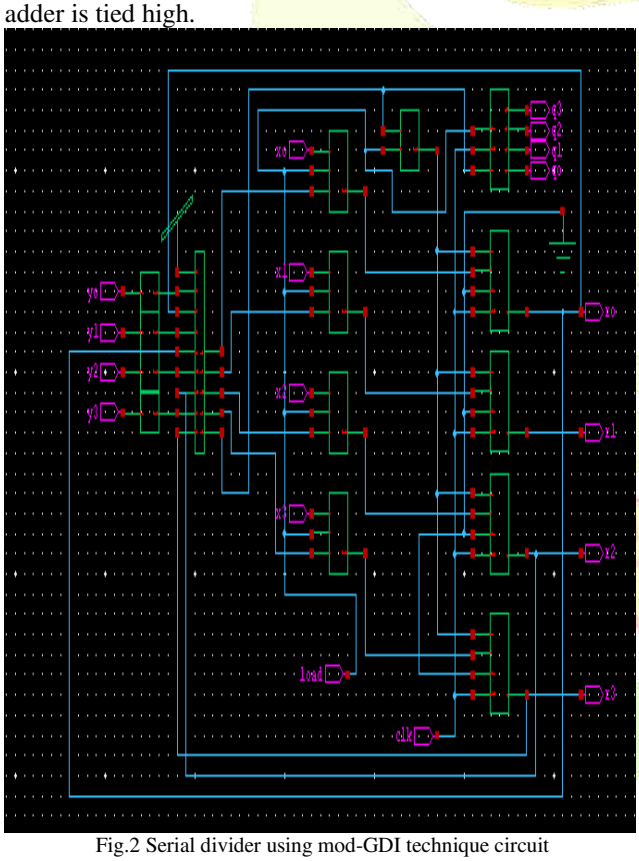

Fig.2 Serial divider using mod-GDI technique circuit

So after the first clock we get X – Y at adder output which is stored in data register. The counter output is incremented to 0001. In the next clock cycle we are subtracting Y from (X – Y), if (X –Y) > Y and counter output will increment to 0010. In the third clock cycle we are subtracting Y from (X- 2Y), if (X -2Y) > Y and counter output will increment to 0011. In this way subtraction continues till carry output of the adder is high.

The register and counter are disabled when carry output of the adder is low and counting will be stopped. Thus the output of the counter ($Q_3Q_2Q_1Q_0$) is equal to the quotient and output from the data register is equal to the remainder (R3, R2, R1, R0).The comparison table shows the analysis of CMOS and GDI technique.

TABLE 1
COMPARISON OF SERIAL AND MOD-GDI TECHNIQUE

A .Carry lookahead adder

There are several technique employs the principle of carry lookahead logic [2]. The construction of a four-bit adder with a carry lookahead scheme is shown in Fig.3. Each sum output requires two exclusive-OR gates. The output of the first exclusive-OR gate generates the Pi variable, and the AND gate generates the Gi variable. The carries are propagated through the carry lookahead generator and applied as inputs to the second exclusive-OR gate. All output carries are generated after a delay through two levels of gates. Thus, outputs S1 through S4 have equal propagation delay times. Gi is called a carry generate, and it produces a carry of 1 when both Ai and Bi are 1, regardless of the input carry Ci. Pi is called a carry

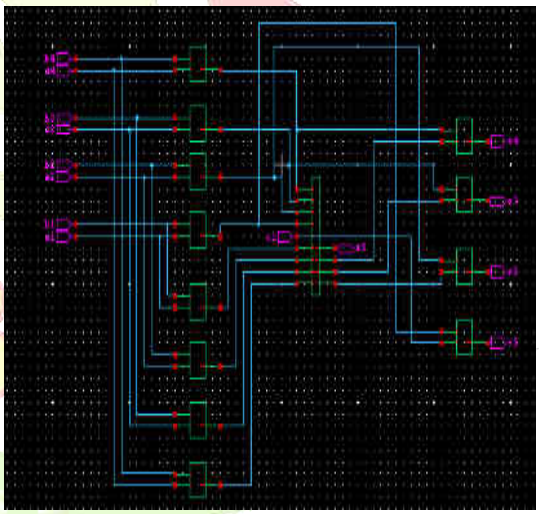

Fig.3 Carry lookahead adder circuit using mod-GDI technique

propagate, because it determines whether a carry into stage i will propagate into stage i+1. This circuit can easily be derived by the equation substitution method. The equations are,

C0= input carry

C1=G0+P0C0

C2=G1+P1G0+P1P0C0

C3=G2+P2G1+P2P1G0+P2P1P0C0

Type	Transistor count	Power consumption	Tool analysis time
CMOS serial divider	964	8.068mW	61.17s
Mod-GDI serial divider	524	0.3861mW	8.91s

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C4=G4+P4G3+P4P3G2+P2P3P4G1+P1P2P3P4C1

By using this equation the carry lookahead adder can be implemented. Here the total propagation time is equal to the propagation delay of typical gate, times the number of gate levels in the circuit.

B. 2:1Multiplexer

The multiplexer [8] is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. When s=0, out=a and when s=1, out=b. It is shown in the Fig.4.A two-to-one-line multiplexer connects one of two 1-bit sources to a common destination.

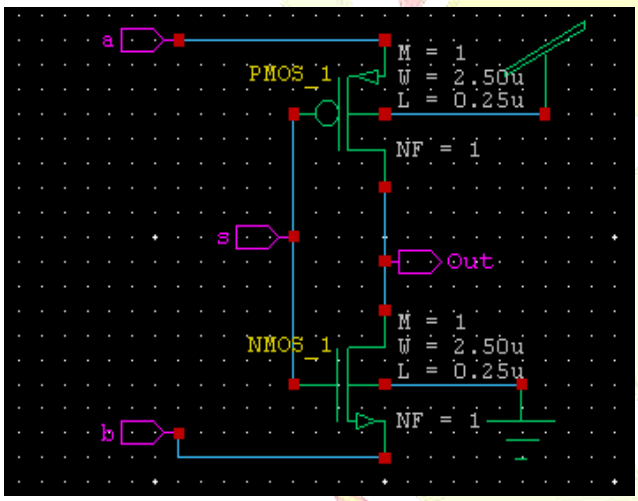

Fig.4. 2:1 multiplexer using mod-GDI technique

C. D Flip Flop

The construction of a D flip-flop[5] with two D latches and an inverter. The first latch is called the master and the second the slave. The circuit samples the D input and changes its output q only at the negative edge of the synchronizing clock. When the clock is 0, the output of the inverter is 1. The slave latch is enabled, and its output q is equal to the master output Y. The master latch is disabled because the clock equal to zero. When the input pulse changes to the logic-1 level, the data from the external D input are transferred to the master[3]. The slave is disabled as long as the clock remains at the 1 level, because its enable input is equal to 0.Any change in the input changes the master output at Y, but cannot affect the slave output. The master slave D flip-flop is shown in the Fig.5. When the clock pulse returns to 0, the master is disabled and is isolated from the D input. At the same time, the slave is enabled and the value of Y is transferred to the output of the flip-flop at q. Thus, a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0.

The behaviour of the master-slave flip-flop is described as

- The output may change only once.
- A change in the output is triggered by the negative edge of the clock.
- The change may occur only during the clock's negative level. The value that is produced at the output of the flip-flop is the value that was stored in the master stage immediately before the negative edge occurred.

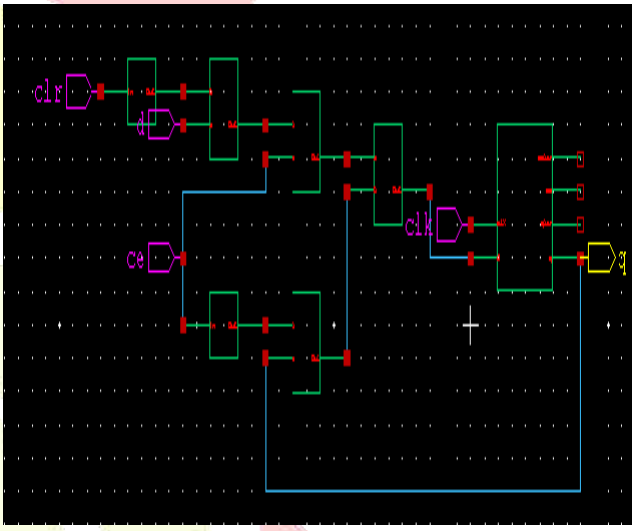

Fig.5 D flip-flop using mod-GDI technique

D. Counter

The synchronous 4-bit up Counter [3] has 3 AND gates, 4 XOR gates and 4 master-slave D flip-flops. Same clock pulse is given to each flip-flop. So with every clock pulse the counter counts one step up. It is an up counter and starts from 0000.Then with each clock pulse counts like 0001,0010,0011,0100 up to 1111.Then it starts from 0000 again. It is a master slave configuration, it actually stores the input at rising edge and it is given to the output at the falling edge of the clock. So the output is noted in the falling edge of the clock. The synchronous up counter is shown in the Fig.6.

There are two additional inputs in the counter, count enable and clear.

- Count Enable input: If count enable is equal to zero, then counter stops counting. If the count enable is equal to 1, each clock pulse results in a counting action.
- Clear input: If clear is equal to one. Then the counter output clears to 0000. If clear is equal to zero, each clock pulse results in a counting action.

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The control logic of the counter is as follows: The XOR gate inverts each bit. The AND chain causes inversion of a bits toward least significant bit is equal to 1. The count enable forces all outputs of AND chain to zero to hold the state.

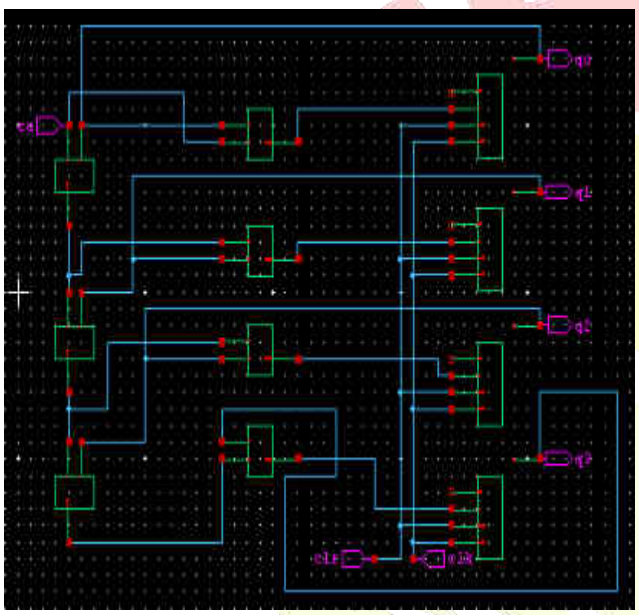

Fig.6 Synchronous 4-bit up counter using mod-GDI technique

E. Simulation results

The serial divider consists of the dividend as 1111 and divisor as 1111 in the input. Then the quotient is one and the remainder is zero is shown in the Fig.7,8.

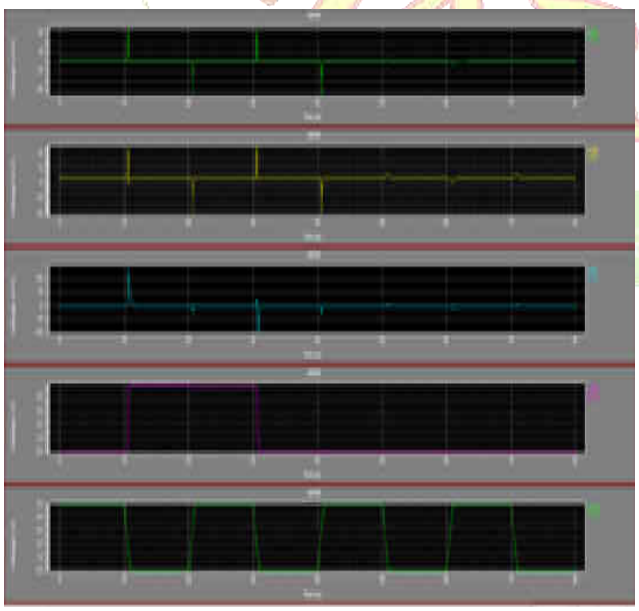

Fig.7 Quotient output of mod-GDI serial divider

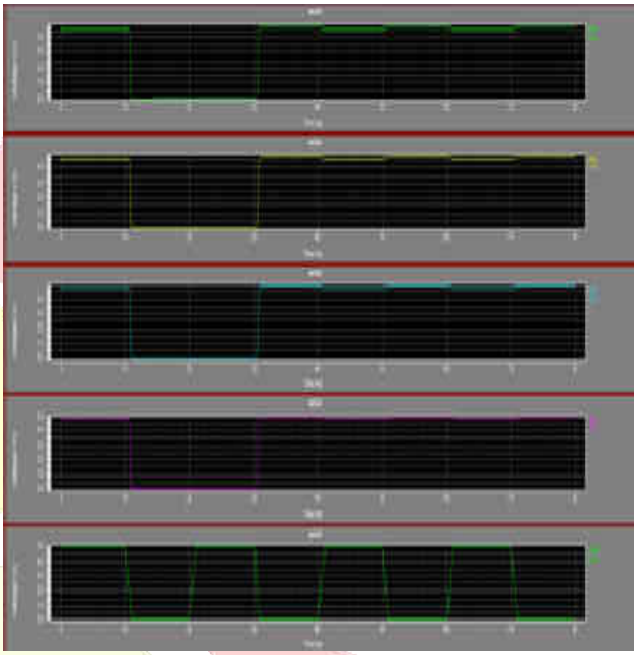

Fig.8 Remainder output of mod-GDI serial divider

III. Discussions

The simulated results confirm the results of serial divider using mod-GDI technique as spitted in Table I. Power consumption as well as area reduction are among few major achievements in this new technique. The problem of low logic level can be reduced by the mod-GDI technique. The system may find its wide application in Arithmetic unit of the high processors.

IV. Conclusion

In this paper, serial divider using mod-GDI technique has been implemented, simulated and analyzed. The performance of serial divider is assessed in terms of area, tool analysis time and power consumption. According to the estimations done, the transistor count, Tool analysis time, power consumption of serial divider using CMOS technology was found to be 964, 61.17s, 8.068mW and the Modified GDI technique was 524, 8.91s, 0.386mW.The designs are simulated using the Tanner EDA tool .Thus we present the design and implementation of serial divider which is optimized in terms of area. Mod- GDI technique is significantly advantageous over other techniques.

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