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A Novel LUT Using Quaternary Logic

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Abstract- in a Very Large Scale Integration (VLSI) circuit, interconnection plays the dominant role in every part of the circuit nearly 70 percent of the area depends on interconnection, 20 percent of the area depends on insulation, and remaining 10 percent to devices. The binary logic is limited due to interconnect which occupies a large area on a VLSI chip. In this work, the designs of quaternary-valued logic circuits have been explored over Multi-Valued Logic (MVL) due to the following reasoning. An approach to mitigate the impact of interconnections is to use quaternary logics, hence, more information can be carried in each wire, reducing the routing network. Therefore, a single wire carrying a signal with N logic levels can replace [$\log_2$N] wires carrying binary signals. Our new method overcomes convectional techniques with simple and efficient decoder logic which reduces the power and area. Using 180 nm CMOS (Complementary Metal Oxide Semi-Conductor) technology reduced power of about 12.32mW Earlier decoder has the power of 41.88mW. Thus the new convectional techniques reduce the average power more than half when compared to the previous techniques. The new proposed decoder has reduced gate which reduces the power consumption. Simulation results demonstrate the effectiveness of the proposed framework in minimizing the power and number of gates. The proposed method is designed using CADENCE virtuoso environment.

Keywords: Multiple-value Logic, Quaternary logics, Look- up tables, FPGAs, Standard CMOS Technology

I. INTRODUCTION

Power dissipation mainly occurs due leakage current and static power dissipation and has formula

$$P_d \propto CV^2_{dd}$$

Therefore by reducing the capacitance value we can able to reduce the dissipation.one of the important advantage of quaternary logic is that has the reduced noise margin when compared to the conventional binary logic. More over if we use the current mode we have to face the problem in the fabrication process and has the high power consumptions.

In General Look-Up Tables (LUT) are basically memories, which implement a logic Function according to their configuration. Configuration values C = (c0….. ci, c_{k-1}); are initially stored in the look-up table structure, and once inputs are applied to it, the logic value in the addressed position is assigned to the output.

II. Binary and Quaternary Look-Up Tables:

The capacity of a LUT |C| is given by

$$|C| = n \times b^k \qquad (1)$$

Where n denotes the number of outputs, k denotes the number of inputs and b for the number of logic values. For

example, a 4-input binary look-up table with one output is able to store $1 \times 2^4 = 16$ Boolean values.

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A binary function implemented by a Binary Look-Up Table (BLUT) is defined as f: $B^k \rightarrow B$, over a set of variables X = (x0,…xi,…. ; x_{K-1}), where each variable xi represents a Boolean value. The total number of different functions |F| that can be implemented in a BLUT with k input variables is given by[1]

$$|F| = b^{|C|} \qquad (2)$$

Where b = |B| (b = 2 in the binary case). For example, a look-up table with 4 inputs (k = 4) can implement one of |F| = 65,536 different functions. Quaternary functions are basically generalizations from binary functions. This function implemented by a quaternary look-up table (QLUT) is defined as g: $Q^k \rightarrow Q$, over a set of quaternary variables Y = (y0,….. yi …… y_{k-1}), where the values of a variable yi, as the values of the function g(Y), can be in Q= {0,1,2,3}. As in the binary case, the number of possible function in QLUTs is given by (2), where b = 4. In this case, the number of functions that can be represented is everywhere 4.3×10^9 for a QLUT with only two quaternary inputs (k = 2), which is much larger than for the BLUT[2].
The quaternary variable y is capable of representing twice as much information as a binary variable x, we note that the cardinality of |Q| = 2 × |B| in our experiments.[3] In other words, two binary variables with the same inputs can be grouped in order to represent a quaternary variable. Such procedure mainly for reducing both the total number of connections and the number of gates. Section I describes the importance of quaternary logic. Section II,III describes the implementation of quaternary logic. . Section IV describes the Quaternary LUT . Section V describes the results and discussion.

III. QUATERNARY LOGIC AND REFERENCE VOLTAGES LEVELS.

This design was implemented using a standard CMOS technology, a single supply voltage and a clock boosting technique to incorporate a 16 to 1 multiplexer and a dual quaternary decoder[4],[5],[6]. One of the most important feature that was taken into account was the area usage since that, in order to perform more complex functions, this circuit needs to be replicated a millions of times in the FPGA

The circuit depicted in the table below has two quaternary inputs, QA and QB, which are then computed by the dual quaternary decoder into the QLUT's binary control signals, B00-B33. The multiplexer 16-to-1 consists of sixteen NMOS switches enhanced with a clock boosting technique[7],[8]. When one of the control signals is high, the corresponding QLUT's line- switch- is activated connecting the corresponding QLUT's quaternary input to the output

Table 1: The four voltage levels

value	Voltage value [v]
0	0
1	0.404
2	0.707
3	1.2

.

A quaternary variable can assume four different logic levels. Assuming a rail-to-rail voltage range and equal noise margins for the four logic levels, three different reference voltage values are required, 1⁄6*V*DD, 3⁄6*V*DD, and 5⁄6*V*DD, to determine a quaternary value[9],[10],[11].A LUT is an array indexing operator,

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where the output is mapped by the input, based on the configuration memory[12]. The configuration values are initially stored in the LUT configuration memory, and according to the input, the logic value in the addressed position is assigned to the output.

1V. 16-1 MUX

A Multiplexer has many inputs and one output has to be selected. Although, the Use of quaternary logic helps to reduce the number of interconnecting wires, which leads to a compact layout, with reduced routing capacitance. We used the typical value for a binary FPGA (10 pF), since it maintain same number of wires, we can increase the number of functions in FPGA [13]When compared to binary quaternary implementation of 16-1 multiplexer quaternary had the least number of gates. For the binary implementation nearly 30 transmission gates are used but in case of quaternary only 24 transmission gates are used as shown in fig. 3 and fig. 4

Table 2: Quaternary and binary input table.

BINARY					QUATERNARY		
DC	8	4	2	1	DC	**4**	**1**
0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	1
2	0	0	1	1	2	0	0
3	0	1	0	0	3	0	1
4	0	1	0	0	4	1	0
5	0	1	0	1	5	1	1
6	0	1	1	0	6	1	0
7	0	1	1	1	7	1	1
8	1	0	0	0	8	2	0
9	1	0	0	1	9	2	1
10	1	0	1	0	10	2	0
11	1	0	1	1	11	2	1
12	1	1	0	0	12	3	0
13	1	1	0	1	13	3	1
14	1	1	1	0	14	3	0
15	1	1	1	1	15	3	1

1V.1 Clock Boosting Techniques

Clock boosting techniques is the important technique for reducing the interconnection problems and increase the speed with reduced delays [14], [15], [16] as in Fig.1.

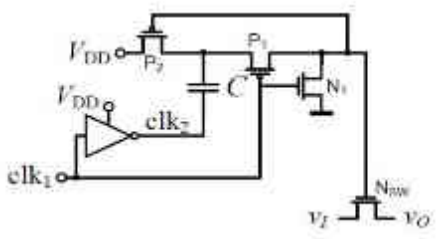

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Fig.1. Proposed transistor-level schematic

Assuming that the capacitor *C* is discharged and clk1 is set to logic 1 (*V*DD), *N*1 turns on and connects node B to ground, while *P*1 turns off and ensures a high impedance path between the nodes A and B. Simultaneously, *P*2 is on and gradually charges the capacitor (and node A) to *V*DD. When clk1 commutes to a logic 0 (ground), *N*1 turns off; the inverter ties the capacitor bottom plate to *V*DD and *P*2 turns off; node Arises to 2*V*DD and *P*1 is turned on connecting node B to 2*V*DD as wanted [17],[18].

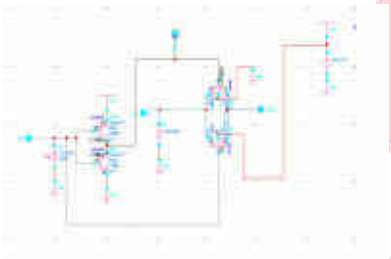

Fig 2: Transmission gate diagram

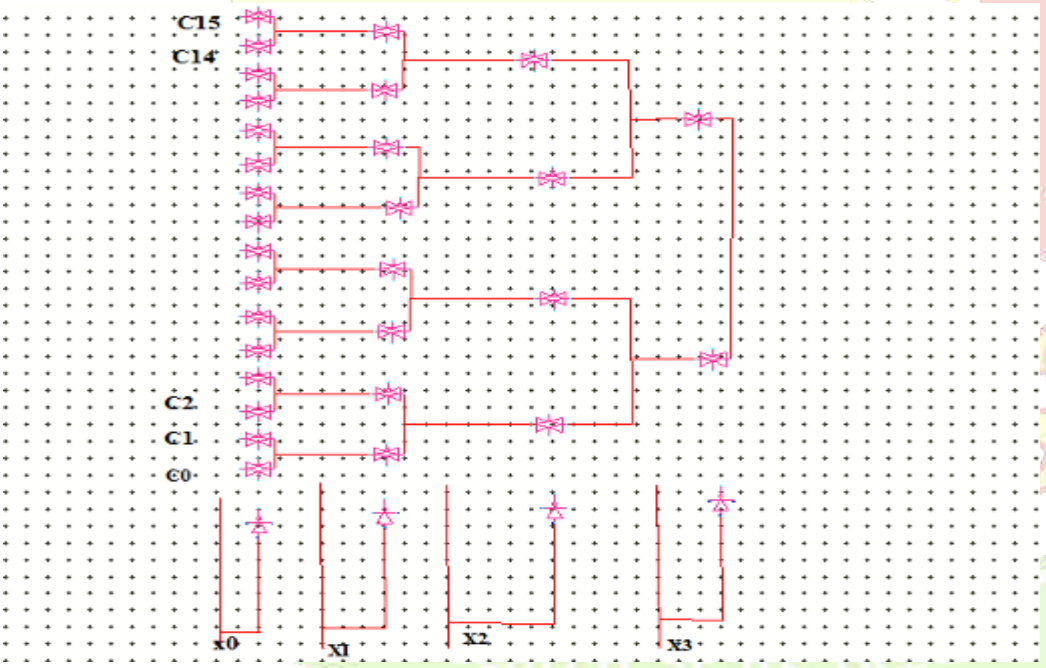

Fig. 3 Binary 16-1 mux

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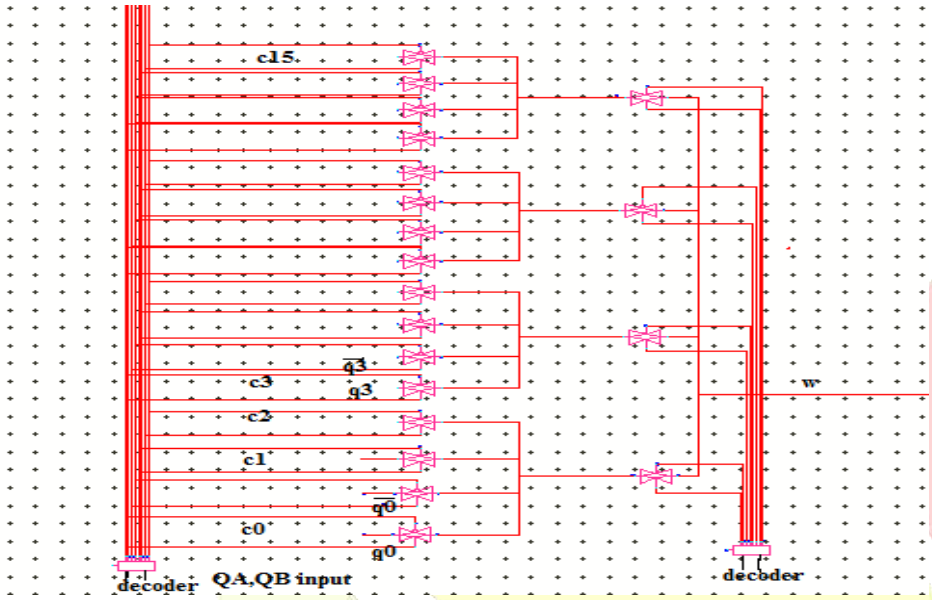

Fig. 4 Quaternary 16-1 mux

From the fig 5 and fig 6 the number of transmission gates has been reduced more number of gates has been used in binary logic whereas less number of gates has been used in quaternary logic when compared to the binary logics [20].

IV.2 QUATERNARY-TO-BINARY CONVERTER

Table 3 the Q-decoder behavior as a function of the quaternary logic value at the input.

Q	Q_0	Q_1	Q_2	Q_3
0_4	1_2	0	0	0
1_4	0	1_2	0	0
2_4	0	0	1_2	0
3_4	0	0	0	1_2

From the above table it shows the binary output as the function of quaternary input. Here Q0, Q_1, Q2, Q3 are the binary values meaning 0 (0V) or 12 (VDD).and q is the quaternary logic as in Fig. 5.

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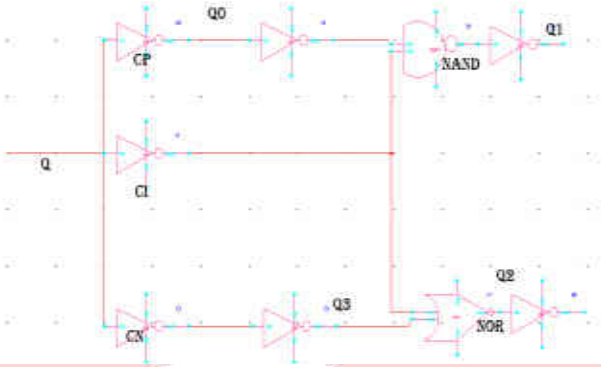

Fig. 5 the Q-decoder logic structure.

The main advantage of this structure compared to previous proposed implementations is that it has standard CMOS structures. The Q-decoder is composed of two comparators CP and CN, and other traditional digital circuits inverters, NANDs and NORs.The CP and CN are self-reference analog comparators shown in Fig. 3. With these structures we are able to detect the four possible voltage levels. In a binary implementation, an inverter may be seen as a comparator where the voltage reference is VDD=2. [19]For our quaternary device, we need three voltage references in order to determine a quaternary value, at 1/6VDD, 3/6VDD and 5/6VDD, as depicted in Fig. 6 given below.

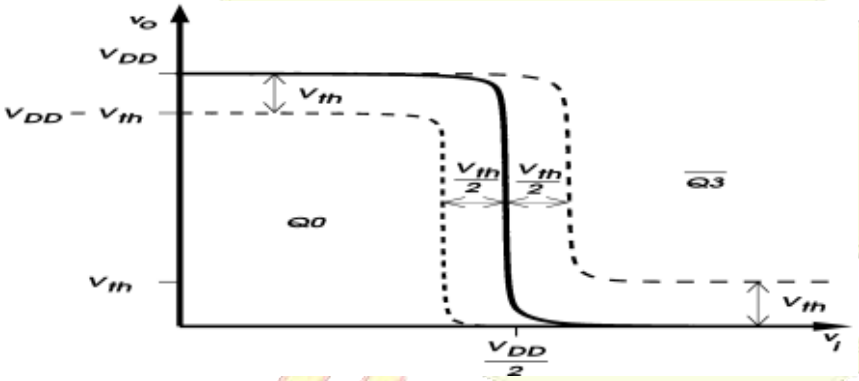

Fig. 6 CP and CN transfer functions.

Thus first for design of decoder we need to design the three
CP, CI, CN .CI is the inverter with the input 1 to get output 0 as in Fig. 7

Fig. 7 a)Cp diagram b) CN diagram

We also implemented the complete binary and quaternary look-up tables with the UMC 130nm technology in order to evaluate their performance and power consumption and the development of the binary and quaternary LUTs was performed. Transistor widths were kept to the minimum value in order to have a

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fair comparison between binary and quaternary versions. The modified quaternary LUT uses less number of gates for NAND and NOR function which results Furthermore, this switch requires two control signals, which increases even more the power consumption and increases the size and complexity on the decoder. Both techniques were evaluated by designing the circuits for the same conditions, output rise time (1.5 ns),confirming that by employing the CB switch saves 58% in power consumption and 27% in area.

V MODIFIED 16-1 MUX WITH MODIFIED DECODER

Figure 4 shows output for the quaternary to binary decoder designed in CADENCE virtuoso environment and it provides decoded values. This code is fed into the input of CB circuit. Depending upon the binary value the decoded value may be changed. The Virtuoso Schematic Composer is used to create the schematic of our design. In the schematic, it will contain devices (transistors) connected together with nets (wire connections).The average Power has been obtained for the modified decoder as shows in the figure

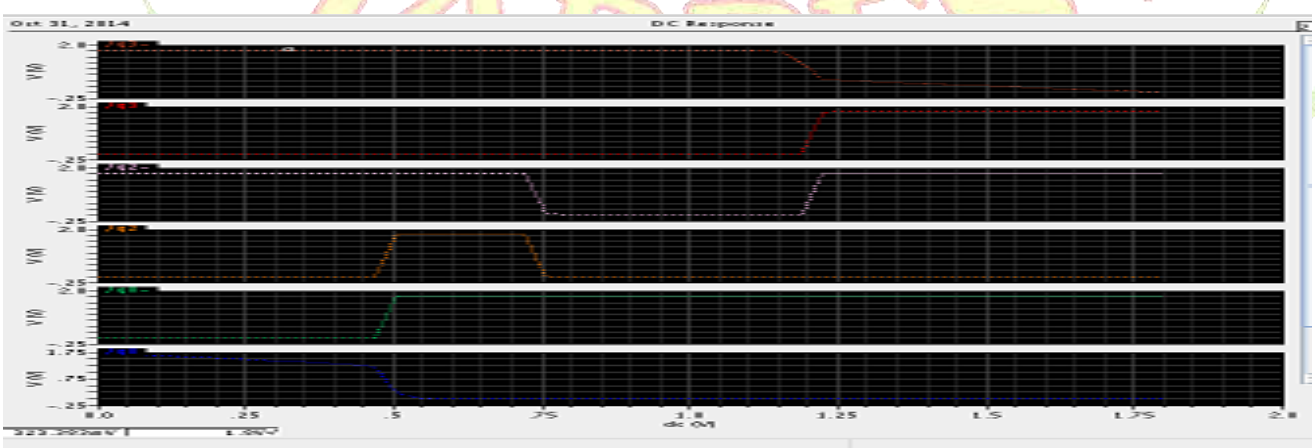

Figure 4.4 Proposed LUT Output Waveform

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NUM OF INPUTS	2	2
LOGIC VALUES	0,1,2,3	0,1,2,3
TECHNIQUES	STANDARD CMOS	STANDARD CMOS
TECHNOLOGY MODE	GPDK 180nm	GPDK 180nm
SUPPLY VOLTAGE	1.8v	1.8v
OUTPUT LOAD	10pF	10pF
NUMBER OF GATES FOR MULTIPLEXER	16	20
NUMBER OF GATES IN DECODER	11	8
POWER CONSUMPTION	12.32µW	41.88µW
NUMBER OF GATES IN FINAL DECODER	22	16
POWER	4.92mW	4.19mW

Thus the below graph figure describes that the proposed quaternary implementation has the reduced number of gates. Reduction in number of gates results in reduced power consumption and hence the overall multiplexer power has been reduced.

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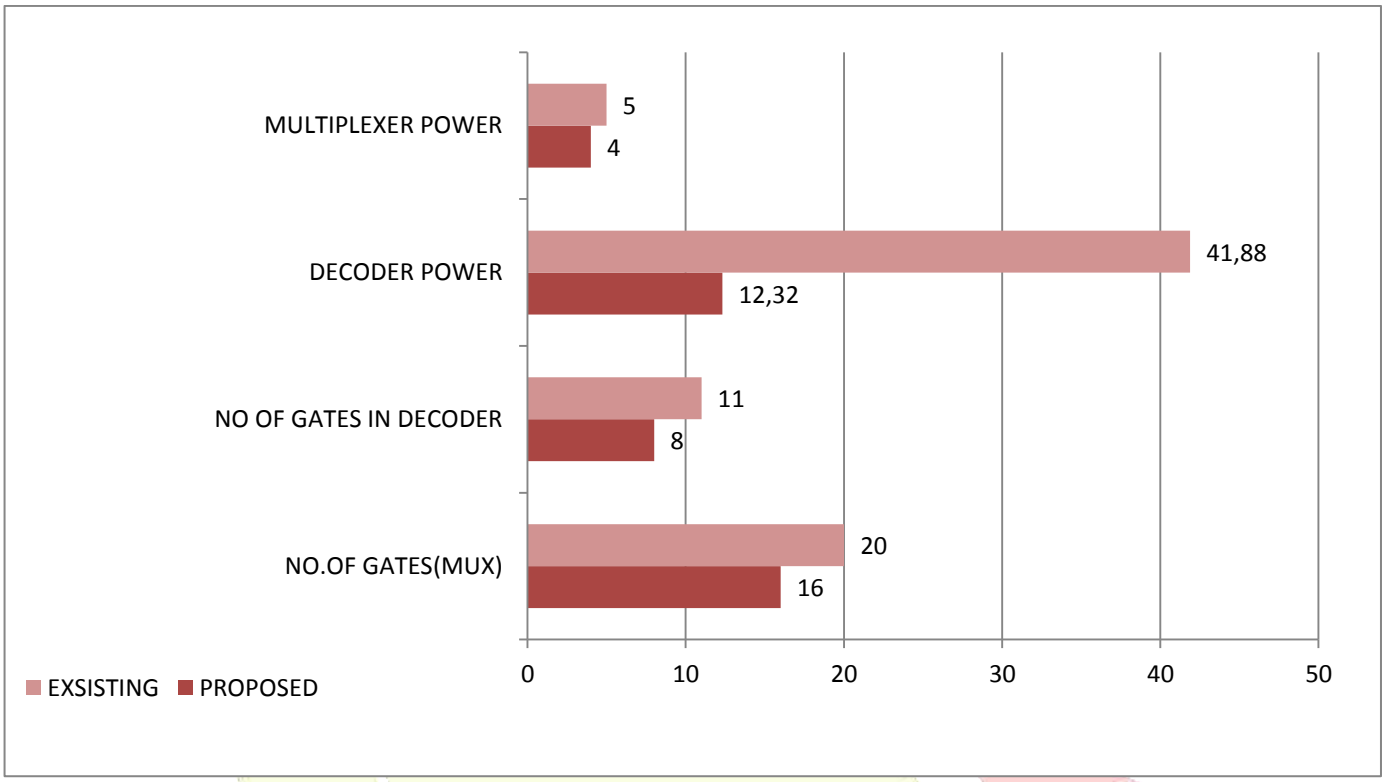

Figure 4.18 Comparison Chart between Existing and Proposed

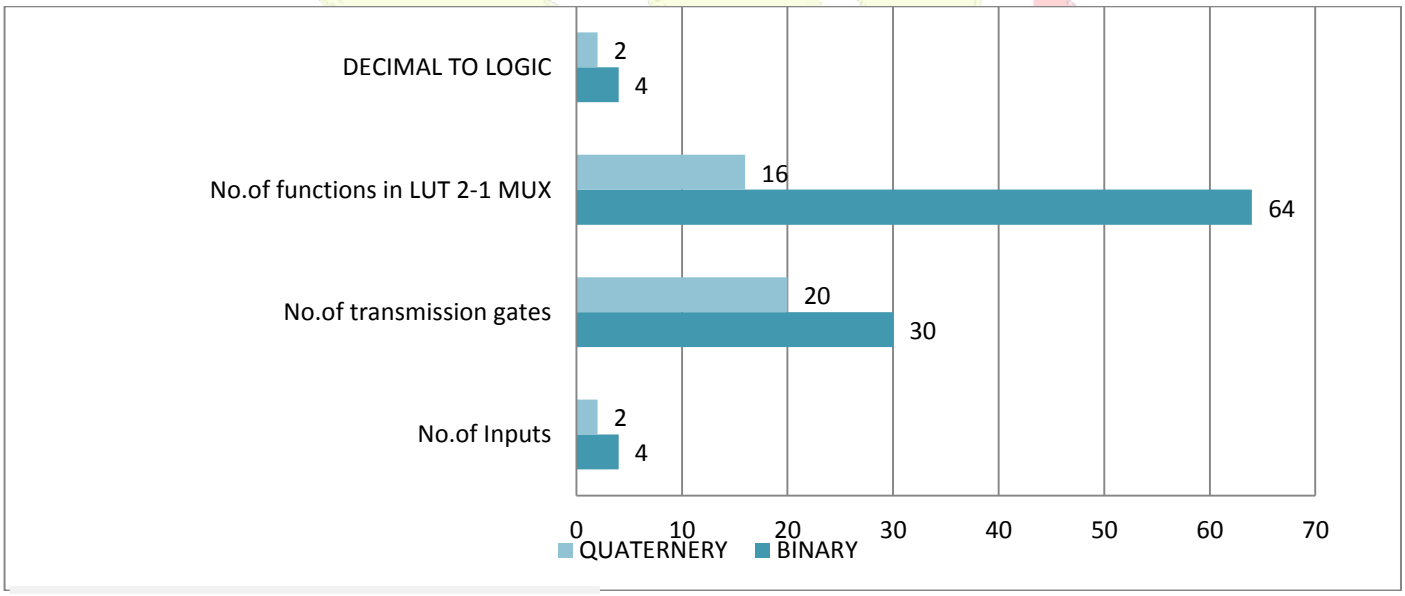

Figure 4.19 Comparison Chart between Binary and Quaternary LUT

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On comparison with the old BLUT with the proposed QLUT has reduces the number of input. Due to the reduced number of inputs interconnection has been reduced which result in less complexity and more functions has to be implemented in the LUT as shown in the Figure 4.19.

CONCULSION

Quaternary logics have many advantages when compared to the binary logics. For the design of QLUT decoder plays the dominant role which converts the quaternary logics to the binary. For the existing system the decoder has the many NAND and INVERTER gates has been used. The new proposed decoder has reduced gate which reduces the power consumption. Simulation results demonstrate the effectiveness of the proposed framework in minimizing the power and number of gates. The proposed method is designed using CADENCE virtuoso environment.

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