ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 10, March 2016

AREA AND DELAY OPTIMIZATION OF BINARY COMMON SUB-EXPRESSION ELIMINATION CONSTANT MULTIPLIER

Viju.R.J1, C.Bagavathi[2]
[1]PG Scholar, Department OF ECE, [2]Assitant Professor, Department of ECE
[1, 2] Sri Krishna College of Engineering and Technology, Kuniamuthur P.O., Coimbatore-641008, Tamil Nadu, India.
[1]r.j.viju5@gmail.com,[2]bagavathic@skcet.ac.in

Abstract*—The main concept of the venture is Reducing the delay and area in VLSI architecture.the efficient VLSI architecture of interpolation filter for multistandard Digital Up Converter (DUC)is implemented by means of two step optimization technique is designed, such that area and delay is reduced. At first, the number of multiplication operation and addition operations are reduced using root-raised-cosine Finite Impulse Response filter for multistandard DUC. By using the constant multiplier number of addition operations are reduced. Shifting operations are performed while considering the constant multiplier. Multipliers are the basic element of any filter like FIR. Hence, a developed 2-bit (BCS) binary common sub-expression based elimination algorithm has been used for designing a constant multipliers. This technique has thrived in reducing the delay, area and power usage and improvement in operating frequency compared to the previously 3-bit BCS-based technique for designing the multi-standard DUC.

***Index terms*— FIR filter, Digital Up Converter, Binary Common Sub-expression**

1. INTRODUCTION

1.1 General

The explosive development in Very Large Scale Integrated (VLSI) circuits in recent years has become the pacing force in the development of new communication systems. In modern telecommunication system the major requirement in communication devices are high data transfer rate and high channel capacity. For satisfying the above requirements, a concept known as Software Defined Radio (SDR) [2] has been introduced. Different problems are faced wile designing VLSI architecture. The circuits designed may be general purpose

integrated circuits such as microprocessor, digital signal processor and memories. They are characterized by a wide range of applications.

The most important entities are, speed, area, delay, design time and power dissipation.

1.2Software Defined Radio (SDR)

Software Defined Radio (SDR) [2] is a radio communication system where components that have been typically implemented in hardware instead of implemented in software on embedded system. SDR software performs all of the demodulation, filtering, and signal enhancement. In an SDR system, realized multiple standards in a single chip by providing a programmable channel select filter at the baseband level.

1.3DUC (Digital Up Converter)

The (DUC) Digital Up Converter is a device used to converts digital baseband signal

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 10, March 2016

up to a pass band signal. The input signal is sampled at a comparatively low sampling rate. This baseband signal is filtered and converted in to higher sampling rate and then modulated with a carrier signal generated from the direct digital synthesizer. The DUC can be mostly used in wireless and wired communication systems.

1.4 FIR Filter

A finite impulse response (FIR) [1] filter is a filter structure can be used to appliancenearly any kind of frequency response digitally. An FIR filter is usually appliance by using a series of multipliers, delays and adders to generate the filters output. Filter design is the process of selecting the filters length and coefficients. The lengthier the filter, the more finely the response can be tuned. An FIR filter can produce weighted average of the N most recent inputs.

1.5Canonical Signed Digit (CSD)

CSD is a significant way for encoding a value in a signed digit delegation, which itself is a non-uniquedelegation and allows one number to be represented in different ways. Probability of digit being zero is close to 66% and leads to systematic implementations of add and subtractnetworks. Canonical Signed Digit is obtained by transforming every sequence of zero followed by ones into followed by zeros.

2. EXISTING METHODOLOGY

2.1 Description

To enhance the power consumption, a combination of symmetrical retimed direct form architecture, balanced modular architecture, detached signed processing architecture, and modified (CSD) Canonical Signed Digit technique-based Finite Impulse Response (FIR) filter [5] have been used. Area and power is measured by means of using less number of multipliers for the interpolation. Look Up Tables are used efficiently. An area, delay and power efficient FIR filter [5] by periodical decomposition of Distributed Arithmetic (DA) based on inner-product computation. By using a modified DA technique, high-speed and medium-speed FIR filter architectures are developed. The LUTs are working in parallel for high-speed FIR filter architecture draws a very high current and area consumption.

Common Sub-expression Elimination (CSE) [6] technique, in which multiplication operations are performed by shift and add operations, is known to be most recently used technique. The number of addition operations performs the multiplication operation defines the Logic Depth (LD) of the circuit.

To achieving less hardware footprint with the help of CSE algorithm for implementing higher order digital filters. A low complexity architecture based on Binary CSE (BCSE) algorithm consumes less hardware and power than CSD-CSE method using a common constant/programmable shift-and-add block [6]. Two different types of architecture used for the addition and shift unit,

1. Constant Shift Method (CSM)
2. Programmable Shift Method (PSM)

2.2 Constant Shift Method (CSM)

In coded Shift Method,with the help of LUT the coefficients values are stored. These coefficients are partitioned into groups of 3-bits and used to select the signal from the multiplexers. Various types of multiplexer are required is [n/3], here n is denoted by wordlength of the filter coefficients. With the help of 8-bit coefficient the CSM can be explained in 'h = 0.11111111'. Here, h is the worst case 8-bit coefficients for all the bits are nonzero and needs the addition and shift operation is maximized. Here using 8-bit, that is n = 8, three multiplexers are required.

$Y= 2^{-1} x + 2^{-2}x + 2^{-3}x + 2^{-4}x + 2^{-5}x + 2^{-6}x + 2^{-7}x + 2^{-8}x.$ (2.1)

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 10, March 2016

$h = 2^{-1}(x + 2^{-1} x + 2^{-2} x + 2^{-3} x + 2^{-4} x + 2^{-5} x + 2^{-6} x + 2^{-7} x)$. (2.2)

Then the shift operation is performed by the final shifter. The circuit does notrequired programmable shifters. And 16 bit coefficient wordlength is generated. In (LUT) Look Up Table,the filter coefficients are stored for the sign bit. The first bit is used to represent the integer part of the coefficients remaining bits are used to represent the fractional part of the coefficients. There are 3-bits with 8combination are possible. Mux1 to Mux7 are used.

Output needs to be complemented in Mux7 hence it is a 2:1 Mux. Fewer number of shift and add unit has been proposed in 3-bit BCSE than 4-bit BCSE. Four 2:1 multiplexers is equivalent to one 8:1 multiplexer. In CSM approach, the coefficients are stored in LUT hence coefficient multiplication is not avoided.

2.3 Architecture of CSM

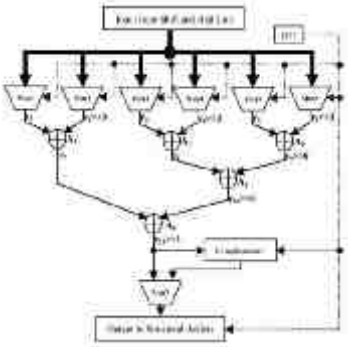

Figure 2.3: Architecture of CSM

2.4 Programmable Shift Method (PSM)

This section shows, reconfigurability is incorporated into BCSE and the filter coefficients are analyzed using BCSE. Resulting coefficients are stored in LUT. Multiplexer units are obtained from the filter coefficients. After considering the number of nonzero operands, the number of multiplexers are selected. Worst case coefficient is defined considering the maximum number of operands.

There are two advantages in this method.The number of addition is reduced compared to CSM and it offers the flexibility of changing the wordlength. The coefficient wordlength of proposed (PSM) Programmable Shift Method architecture reformed dynamically.

2.5Architecture of Programmable Shift Method

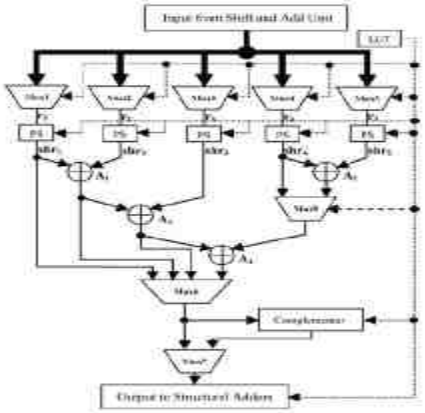

Figure 2.5: Architecture of PSM

2.6 Disadvantages

The major disadvantages of the existing system are listed below:

1. Basedon FIR filter design the (CSM) Constant Shift Multiplication is performed, involves use of redundant adder in the multiplier block. Increasing the number of hardware leads to more area and power consumption, and makes the design unsuitable for SDR [6] system by considering low power and low area consumptions are the key concerns.

2. By compromising the speed of operation power reduction has been achieved that makes the symmetrical retimed direct form architecture inappropriate for the SDR [2] system.

3. PROPOSED METHODOLOGY

3.1 Proposed System

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 10, March 2016

A new reconfigurable architecture has been proposed in this project to overcome the discussed disadvantages,for initial reduction of (MPIS) Multiplications Per Input Sample [8] and Additions Per Input Sample (APIS) [1] and subsequent reduction of hardware and power by designing an effectual constant multiplier using 2-bit Binary Common Sub-expression (BCS). Compared with the 3-bit BCS based constant multiplier design the 2-bit BCS will leads to achieve good propagation delay.

3.2 Architectural Design

The reconfigurable architecture of FIR [2] interpolation filter based on the proposed method is shown below in fig 3.2.

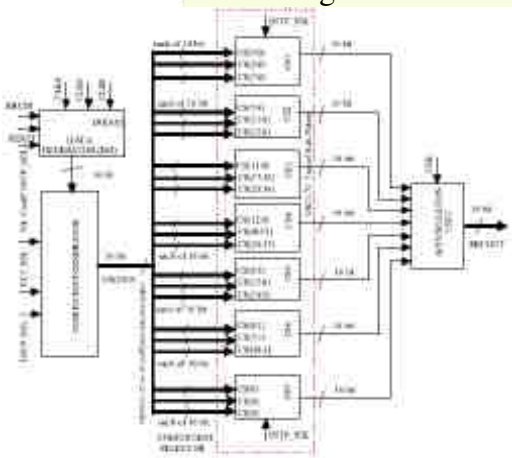

Figure 3.2 Architecture of RRC filter

The proposed reconfigurable RRC filter architecture subsistof thedifferent major modules. They are Data Generator (DG), a Coefficient Generator (CG), a Coefficient Selector (CS) and an Accumulation Unit block (FA).

3.2.1 Data Generator (DG)

Based on the selected value of the interpolation factor selection parameter (INTP_SEL) the input data (RRCIN) are sampled in Data Generator block. 25-, 37- and 49- tap filters with interpolation factors of four, six, and eight compose a branch filter of seven taps. i.e.)

[25/4] = [37/6] = [49/8] = 7

Above equationspecifies that, to create the full filter response seven sub-filters are required for multiplication operation of the filter coefficients with input sequence.

3.2.2 Coefficient Generator (CG)

The Coefficient Generator unit performs the multiplication between the filter coefficients and the inputs. The proposed two phase optimization method helps to reducing the hardware usage by a substantial amount to facilitate reconfigurable FIR filter [5] implementation with low computation time and low complexity.

The Coefficient Generator block flow diagram for programmable coefficient sets is shown below in figure 4.3. The code generator includes the following blocks namely, (FCP) First Coding pass, (SCP) Second Coding Pass,(PPG) Partial Product Generator, Multiplexer Unit (MU) and Final Addition (FA) block.

The functionality of each block represented in fig 3.2.2 is described as follows.

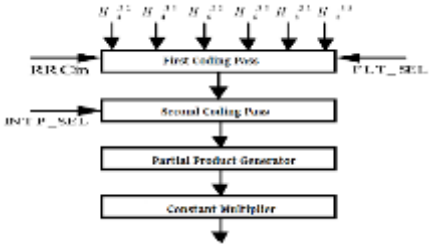

Figure 3.2.2 CoefficientGenerator Block

3.2.3 First Coding Pass (FCP)

The input to the First Coding Pass block are two sets of 25-, 27-, and 49- tap filter coefficients which differ only by roll off factor. Forthe three different interpolation factors inside the FCP block, all the three coding blocks are running in parallel. Matching between all bits is explored

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 10, March 2016

vertically within the two coefficients of same length filter.

The architecture for implementation of First Coding Pass is shown below in fig 3.2.3

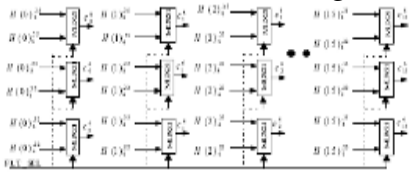

Figure 3.2.3 Architecture of FCP block

In the above First Coding Pass block, the coefficient sets are multiplexed through one 2:1 multiplexer, depending on the roll off factorone (FLT_SEL) control parameter selects the desired filter. This multiplexing method helps to decrease the requirement of the multiplier by half as the total number of coefficients required is 111 instead of the initial requirement of 222.

3.2.4 Second Coding Pass (SCP)

In the (SCP) Second Code Passing, the coefficients obtained from the (FCP) First Coding Pass block are passed through different set of multiplexers; depending on the interpolation factorone(INTP_SEL) control parameter selects the desired filter. The total number of filter coefficients that will process further from the prior requirement of 111 is reduced using above method.

The FCP block output are coded into three different set of coefficients that are 13, 19, and 25 in number and are passed through another CP block to get the final coefficient set. In this block, the common terms present verticallyamongst these three coded coefficient sets have been found out and coded accordingly.

The architecture view of Second code pass block is shown below in fig-3.2.4,

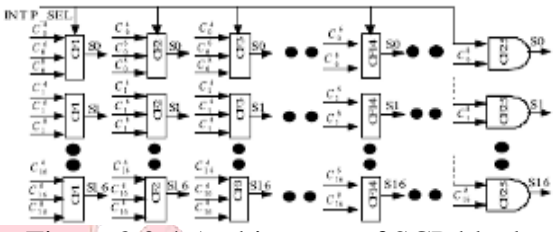

Figure 3.2.4 Architecture of SCP block

The combination of (FCP) First Coding Pass and (SCP) Second Coding Pass steps lessens the requirement of MPIS from 42 to 7 and APIS from 36 to 6, which facilitates 83.3% improvement of this design. (APIS) Addition Per Input Sample and (MPIS) Multiplication Per Input Sample can be further reduced by considering more filters of different specifications.

3.2.5 Partial Product Generator (PPG)

The partial product generator during the multiplication operation between the input data (X_{in}),by using shift and add method,the filter coefficients is generated. In Binary Common Sub-expression Elimination (BCSE)algorithm, realizations of the common sub expression using shift and add method [6]is used to eliminate the common term avail in a coefficient. The architecture for implementation of Partial Product Generator block is shown below in fig 3.2.5.

Figure 3.2.5 Architecture of PPG block

2-bit BCSs stretching from 00 to 11 have been considered. Inside four of these BCSs, an adder is essential only for the decoration 11.This facilitates reduction in hardware and improvement in speed while multiplication operation are performed.

BCSE Technique

Instead of 3 bit BCSE technique, 2 bit BCSE technique [6] is used. In this technique the Logic Depth can be defined as,

ISSN 2395-695X (Print)
ISSN 2395-695X (Online)
International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)
Vol. 2, Special Issue 10, March 2016

LD_{2BCS}= [$Log_2$2] +Log_2 [16/2] =4 (3.1)

Where the term $log_2$2 is due to the two bit BCS and the term log_2 [16/2] is due to 16 bit word length of coefficients. Also the Propagation Delay can be defined as

T_{2BCS}=4 x t_{add} + $t_{4:1mux}$+ t_{acc} (3.2)

Where,$t_{add}$is the delay of every adder used in the constant multiplier.

$t_{4:1mux}$ is the delay for the 4:1 multiplexer.

$t_{acc}$is the delay for final adder in the delay chain of FIR filter.

The 2 bit BCS leads to achieve better propagation delay as compared with the 3 bit BCS based constant multiplier design. In any FIR filter, the multiplication operation [1] between the inputs and the coefficients with word length 16 bits can be given as

$y1=x1+2^{-1}x1+2^{-2}x1+2^{-3}x1 +\ldots+2^{-14}x1+2^{-15}x1$ (3.3)

By considering 2 bit BCS technique i.e.) x2 = x1 + 2^{-1}x1, the above equation (3.3) rewritten as

$y1=x2+2^{-2}x2+2^{-4}x2 +\ldots +2^{-10}x2 +2^{-12}x2 + 2^{-14}x2$(3.4)

In the proposed architecture, the shift and add unit has been grouped in eight preshifted standards of 2*N* + 1 bit, here *N* = 8, 7, 6, 5, 4, 3, 2, 1 to implement the above equation (4.4). This will help in reducing the adder width and multiplexer. As this shifting is done the maximum error due to truncation has been precalculated and added in the ending addition operation of the constant multiplier unit.

3.2.8 Coefficient Selector

In the reconfigurable FIR filter [5], depending on the corresponding interpolation factor the coefficient selector block steer the proper data to the final accumulation unit. The hardware architecture of code selector block is shown below in fig 3.2.8,

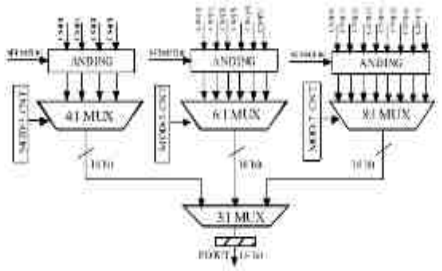

Figure 3.2.8 Hardware architecture of CS block

The output of the Code Generator block is the input to the Coefficient Selector block.

3.2.9 Constant Multiplier

CM (Constant Multiplier)is used to perform the shifting operation between the inputs and coefficients. Number of shifting operation is performed while optimize the number of addition and multiplication operation. Multiplexed coefficient are used for select the output of the partial product unit.

4. SIMULATION RESULT

By comparing both the existing technique using various algorithm with 16 bit area, delay and power has to be improved. Delay, area and power hasbeen minimized. Comparison are shown below,

Table 4: Comparison of simulation outputs

S.NO	PARAMETERS	EXISTING METHOD	PROPOSED METHOD
1	DELAY	16.683 ns	11.703 ns
2	AREA	9,967(gate count)	7,384 (gate count)
3	POWER	53.5 mW	39 mW

5. CONCLUSION AND FUTURE SCOPE

Different problems has been encountered while the reduction of Multiplication Per Input Sample and Reduction Per Input Sample with the help of Constant multiplier. If the constant multiplier is processed, the area and delay should be augmented.Binary Common Subexpression

Elimination methods are implemented in constant multiplier to reduce the addition and multiplication unit.The number of gates has to be reduced for obtaining the minimum area and delay and shifting operation is performed while considering the constant multiplier is processed.A constant addition and multiplication less architecture is used instead of using the coefficient selector Unit. Number of addition and multiplication operation should minimized by using the 2-bit BCSE algorithm with the help of multiplexer unit in the aim of optimizing area and delay.

REFERENCES

[1] D. Shi and Y. J. Yu, "Design of linear phase FIR filters with high probability of achieving minimum number of adders," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, no. 1, pp. 126–136, Jan. 2011.

[2] J. Mitola, "The software radio architecture," IEEE Commun. Mag., vol. 33, no. 5, pp. 26–38, May 1995.

[3] J. Xie, J. He, and G. Tan, "FPGA realization of FIR filters for high-speed and medium-speed by using modified distributed arithmetic architectures," Microelectron. J., vol. 41, no. 6, pp. 365–371, Jun. 2010.

[4] O. Gustafsson, "Lower bounds for constant multiplication problems, "IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 11, pp. 974–978, Nov. 2007.

[5] P. K. Meher, S. Chandrasekaran, and A. Amira, "FPGA realization of FIR filters by efficient and flexible systolization using distributed arithmetic," IEEE Trans. Signal Process, vol. 56, no. 7, pp. 3009–3017, Jul. 2008.

[6] R. Mahesh and A. P. Vinod, "A new common Subexpression elimination algorithm for realizing low-complexity higher order digital filters," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 2, pp. 217–229, Feb. 2008

[7] R. Mahesh and A. P. Vinod, "New reconfigurable architectures for implementing FIR filters with low complexity," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 29, no. 2, pp. 275–288, Feb. 2010.

[8] S.-F. Hsiao, J.-H. Zhang Jian, and M.-C. Chen, "Low-cost FIR filter designs based on faithfully rounded truncated multiple constant multiplication/accumulation," IEEE Trans. Circuits Syst. II,Exp. Briefs, vol. 60, no. 5, pp. 287–291, May 2013.

[9] S.-J. Lee, J.-W. Choi, S. W. Kim, and J. Park, "A reconfigurable FIR filter architecture to trade off filter performance for dynamic power consumption," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 12, pp. 2221–2228, Dec. 2011.