ISSN 2395-695X (Print)
ISSN 2395-695X (Online)

International Journal of Advanced Research in Biology Engineering Science and Technology (IJARBEST)

Vol. 2, Special Issue 10, March 2016

Design of Efficient Content Addressable Memories (CAM) using FINFET Technology

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Abstract — Power dissipation due to memories has become a major concern of modern digital design. The conventional CMOS technology has a major problem of short channel effects. So, the CAM cells are designed using FinFET technology which has better gate control over drain to source current. The CAM has a parallel active circuitry which consumes more power and the main challenge in designing the CAM is to reduce the power consumption without reducing the speed and memory density. This project proposes a hybrid-type CAM for the advantage of speed and performance of the system and the results are compared with conventional CAM cell.

Keywords— Content Adderssable Memory (CAM), Hybrid-Type CAM, high performance, low area, low power, searching, SRAM.

I. INTRODUCTION

Content-Addressable Memory (CAM) searches for matching data by content and returns the address at which the matching data is found. CAMs are used extensively today in applications such as network address translation, pattern recognition, and data compression [1] [2]. In these applications, there is a steady demand for CAMs with higher density and higher search speed, but at constant power. In networks like the Internet, a message such an as e-mail or a Web page is transferred by first breaking up the message into small data packets of a few hundred bytes, and, then, sending each data packet individually through the network. These packets are routed from the source, through the intermediate nodes of the network (called routers), and reassembled at the destination to reproduce the original message. The function of a router is to compare the destination address of a packet to all possible routes, in order to choose the appropriate one. A CAM is a good choice for implementing this lookup operation due to its fast search capability [3].

With the onset of the 22-nm technology node, planar bulk-CMOS has begun losing its long-lasting reign in the semiconductor industry due to severe short-channel effects [4]. Double-gate field-

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effect transistors (DGFETs) are an attractive alternative to planar MOSFETs since two gates enable better electrostatic control over the channel [5]. FinFET, a type of DGFET, has become popular because of its scalability and compatibility with the planar CMOS process.

Internet routers forward data packets from an incoming port using an address lookup function. The address lookup function examines the packet's destination address and chooses an output port associated with that address.

Line No.	Address	Output Port
1	101XX	A
2	0110X	B
3	011XX	C
4	10011	D

Table 1:Simplified Routing Table

The router's list of destination addresses and their corresponding output ports is called the routing table. An example of a simplified routing table is displayed in Table 1.

The router searches for the destination address of each incoming packet in the address lookup table to find the appropriate output port. For example, if the router receives a packet with the incoming address 01101, the address lookup matches both Line 2 and Line 3 in the table. Line 2 is selected since it has the most defined bits, indicating it is the most direct route to the destination. This lookup style is called longest-prefix matching and is required to implement the most recent Internet Protocol (IP) networking standard. In this paper, a recently proposed hybrid-type CAM is proposed to reduce the area, power and increase the performance.

The rest of this paper is organized as follows. Section II describes the literature review. Section III describes an existing method for CAM cell. Section IV describes the proposed method for Hybrid-type CAM. The conclusion is given in Section V.

II. LITERATURE REVIEW

Kostas Pagiamtzis and A. Sheikholeslami,[3] ”Content addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey” proposed the methods for reducing power consumption. The

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main drawback of using this method is, the speed of a CAM comes at the cost of increased silicon area and power consumption .

Igor Arsovski and A. Sheikholeslami,[9] "A mismatch-dependent power allocation technique for match-line sensing in content-addressable memories" proposed the match-line (ML) sensing scheme that allocates less power to match decisions involving a larger number of mismatched bits. This sensing scheme has the disadvantages of requiring a larger energy investment by supplying larger currents.

Kaushik Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand,[10] "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," proposed transistor intrinsic leakage Mechanisms such as the new high-resolution lithographic techniques, new device designs, structures, and technologies should be developed to keep SCEs under control at very small dimensions. This technique has the limitations of strong effect on the band bending over a significant portion of the device.

III. EXISTING METHOD

All CAM bitcells described in the literature have two components: a core memory cell (typically a 6T SRAM cell) for data storage and an XOR/XNOR matching circuitry for data comparison [1]. Based on various designs of core cells and matching circuits, a CAM can be classified into NOR, NAND, and ternary categories [1]. In a NOR CAM bitcell, as shown in Fig. 1, transistors T1–T6 form the core SRAM cell, while transistors T7–T10 form the matching circuit. Using SG and ASG FinFETs in our CAM bitcells, we can generate four possible bitcell configurations: All-SG, All-ASG, Core-ASG, and Match-ASG. As the names suggest, an All-SG (All-ASG) CAM has both core and matching circuits built with SG (ASG) FinFETs. On the other hand, a Core-ASG (Match-ASG) CAM has only the core (matching) circuit built with ASG FinFETs and the rest with SG FinFETs [6].

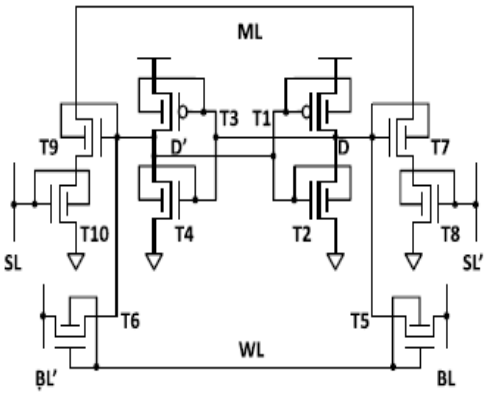

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Fig. 1 Schematic diagram of a FinFET NOR CAM bitcell.

However, since the matching circuit determines the search delay of the CAM and has fewer transistors than the core [1], we do not consider the Match- ASG bitcell in our designs because it is not wise to slow down the CAM only to save a small fraction of the total leakage power. Though the above configurations are also possible for NAND and ternary CAMs, we choose the NOR CAM as a reference for our designs.

Every CAM bitcell in an array has a match line (ML) and a pair of complementary search lines (SLs) running in mutually perpendicular directions, to implement the data search operations [1]. As part of the core SRAM cell inside the CAM bitcell, the wordline (WL) and bitlines (BLs) run in the same direction as the ML and SLs, respectively.

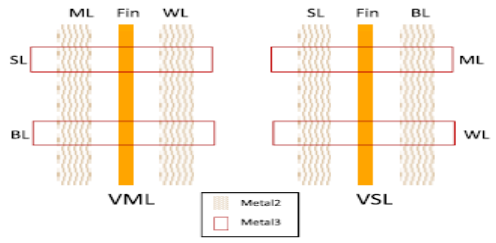

Fig. 2 Layout styles of VML and VSL.

We consider the direction of the parallel fins in the FinFET layouts as our reference direction. This also happens to be the direction of the power lines (VDD and GND). Hence, there are two ways in which ML/WL and SL/BL can run in bitcell layouts based on the reference direction, as shown in Fig. 2. When ML/WL run in metal2 (M2), parallel to the fins, and SL/BL run in metal3 (M3), perpendicular to the fins, we refer to it as a vertical- ML or VML CAM. When ML/WL run in metal2 (M2), parallel to the fins, and SL/BL run in metal3 (M3), perpendicular to the fins, we refer to it as a vertical- ML or VML CAM. The layout of a VML NOR-CAM bitcell is shown in Fig. 3(a).

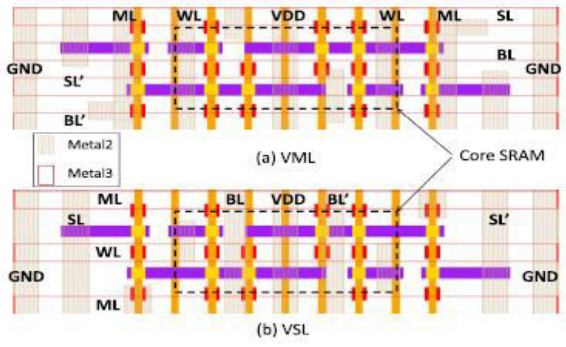

Fig. 3 Layout styles of NOR CAM cell (a) VML (b) VSL

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When SL/BL run in M2, parallel to the fins, and ML/WL run in M3, perpendicular to the fins, we refer to it as a vertical-SL or VSL CAM. The layout of a VSL NOR-CAM bitcell is shown in Fig. 3(b).

As the M3 lines (i.e., SLs in VML and ML in VSL) are longer than the M2 lines in the CAM bitcell layouts (Fig. 3), and also typically wider, they are likely to accumulate larger parallel-plate capacitance than M2 lines. In a typical CAM application, such as an Internet router, ML and SL capacitances undergo switching transitions in every search cycle, and dominate the total dynamic power. Therefore, careful capacitance-aware layout design is important for dynamic power optimization of CAM arrays.

IV. PROPOSED HYBRID-TYPE CAM DESIGN

Hybrid-type CAM design has two types of arrays, NOR-type array with XOR CAM cell and NAND type array with XNOR CAM cell. Both array has the advantages of performance and power of the system. Hybrid-type CAM structure consists of SEG1, SEG2 and CONTROL circuitry. In SEG 1, the circuit is designed using XNOR type and then the pull-down transistors are arranged using NAND-type. In SEG 2, the, the circuit is designed using XOR type and then the pull-down transistors are arranged using NOR-type. The Hybrid-type CAM structure is shown in Fig. 4

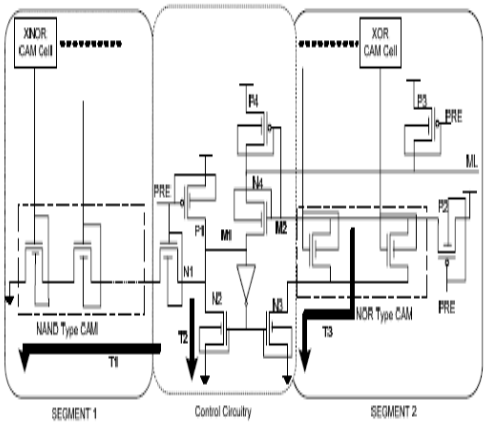

Fig. 4 Hybrid-Type CAM Structure

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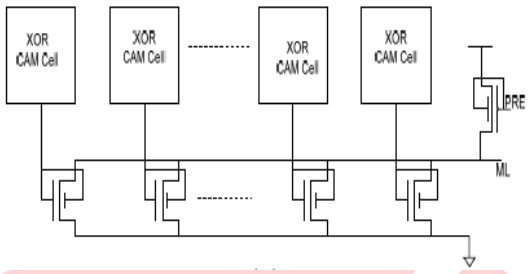

Fig. 4(a) NOR Type CAM array

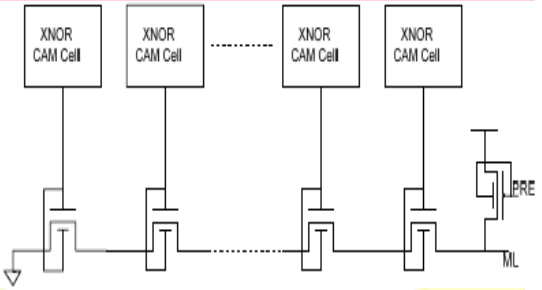

Fig. 4(b) NAND Type CAM array

Search operation of Hybrid-type CAM cell

In case of searching a data, the input data is compared with that of stored data. The search operation of CAM cell is performed in two phases ML precharge and ML evaluation. In ML precharge phase, match line is charged to high and then in ML evaluation phase based on the match and mismatch of the words the match line will change the logic from high to low or low to high.

a) ML Precharge phase

During the precharge phase, the PRE signal is low and the Match Line (ML) is charged to high through P3. In Fig 4, T1, T2 and T3 are the pull-down paths in the circuit. The M1 node is at high because of transistor P1, which drives the transistors N2 and N3 OFF due to which the path T2 and T3 are disconnected from ground. The low PRE signal turns OFF transistor N1. Therefore all the pull-down paths are disconnected.

b) ML Evaluation Phase

During evaluation phase, the PRE signal is high and the search bits are loaded on bit lines. The hybrid-type CAM is divided into two segments SEGMENT-1 (SEG_1), and SEGMENT-2 (SEG_2) as shown in the Figure 4. When two segments have match, then match line will discharge through any one of the pull-down paths. When we search the data we come across 4 different cases

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but the exact matching occurs only when both the segments are matched. The voltages of each node are shown in Table 2. The detailed explanation of this matching process is given below.

Case i): In this case, the SEG1 is mismatched and SEG2 is mismatched or matched. Since the SEG1 is mismatched there exists no discharge path because there may be at least one transistor that is OFF. So the node voltage M1 remains HIGH. Thus in this case the matching process does not depend on the SEG2. Since there is no discharge path the Match-line still remains in the HIGH state.

Case ii): In this case, SEG1 is matched and SEG2 is mismatched. As the SEG1 is matched all the transistors that are connected in the NAND fashion are in ON state, so that there exists a discharge path through the path T1. And thus, the node M1 remains LOW and the two pull-down transistor P5 gets ON and so, there exists a path T2 to discharge. Now as the SEG 2 is mismatched there exists at least one path to discharge through N3 so that the node M2 remains LOW. Hence in this case, there won't be any path to discharge the match-line.

Case iii): In this case, both the segments are matched. Thus, as the SEG1 is matched, the node M1 gets LOW value as there exists a discharge path. Now in case of SEG2, as it is matched all the transistors are turned OFF and the path T3 to ground is disconnected. Now the node M2 is at HIGH state making the transistor N4 to turn ON. Now there exists a path for Match-line to discharge the data, through the paths T1 or T2. As the path T2 is the fastest path to discharge the data, the Match-line discharges through the transistor P5. Thus it indicates that the data have been matched properly. In this design as we have two pull-down paths to discharge the match-line. It discharges through path T2 as path T1 has transistors connected which takes long time to discharge. Thus, this design provides better performance.

	SEG 1	SEG 2	Path			Key Node			Result
			T1	T2	T3	M1	M2	ML	
Case 1	Mismatch	Mismatch	X	X	X	H	H	H	Mismatch
	Mismatch	Match	X	X	X	H	H	H	Mismatch
Case 2	Match	Mismatch	0	0	0	L	L	H	Mismatch
Case 3	Match	Match	0	0	X	L	H	L	Match

Table 2: Node Voltages of each node of Hybrid-type CAM Cell.

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V. SIMULATION RESULTS

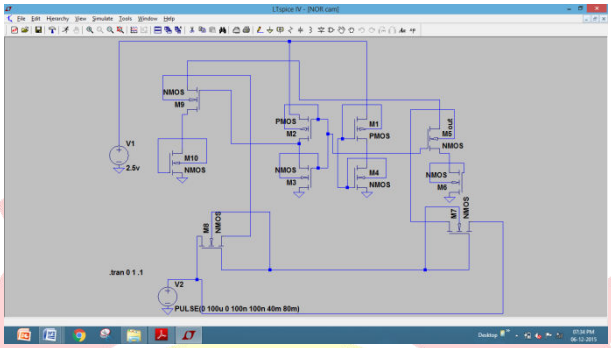

Fig. 5.1 Circuit diagram of NOR CAM cell

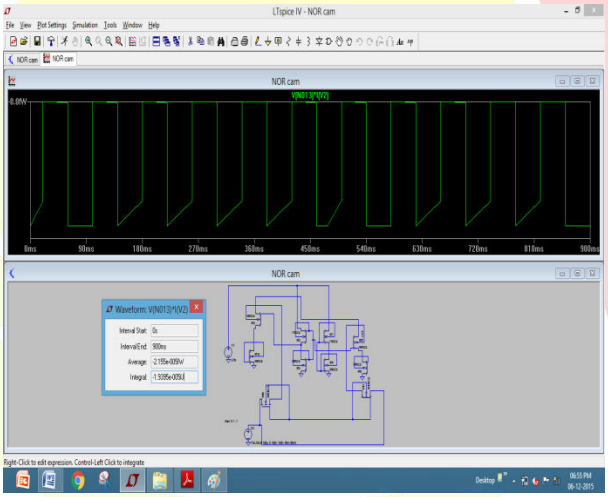

Fig. 5.2 Waveform of input pulse with its average power

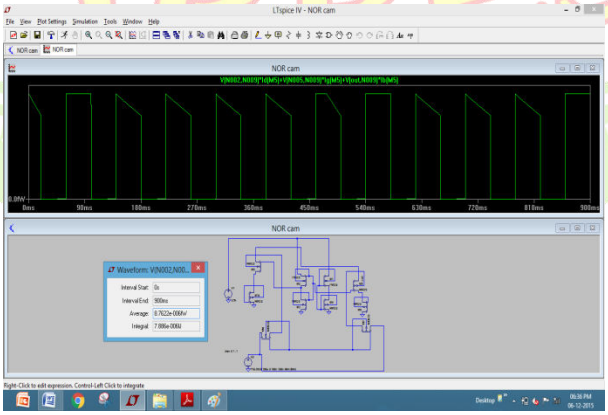

Fig. 5.3 Waveform of output pulse with its average power

VI . CONCLUSION

In this paper, we have designed a Hybrid-type CAM using FinFET technology for the advantages of low power, low area and high performance of the system. Further the energy (power & delay product) saved through this hybrid-type CAM is more when compared to the existing CAM. Here, the hybrid-type CAM uses a 4T cell instead of using 10T cell. Due to this, the area gets reduced and finally power also gets reduced.

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